Session 9A: New Developments in Logic Representation and Verification Techniques

Moderators:

H. Eveking, University of Frankfurt, Germany and
L. Claesen, IMEC/Katholieke Universiteit Leuven, Belgium

The first paper analyses decision diagrams. The second paper applied learning techniques in verifying combinational circuits. The third paper extends BDDs.

How Many Decomposition Types Do We Need?
B. Becker and R. Drechsler

VERIFUL: VERification Using FUnctional Learning
R. Mukherjee, J. Jain, and M. Fujita

Implicit Manipulation of Polynomials Using Zero Suppressed BDD
S. Minato