Session 7C: Self-Checking Approaches
Moderators:

J. Figueras, Universidad Politecnica de Catalunya, Spain and
M. Bushnell, Rutgers University, USA

The Session concerns concurrent error detection techniques including self-checking implementations for RAMs and FFT as well as off-line and/or concurrent checking for bridging and parametric faults based on intermediate voltage monitoring.

Area Versus Detection Latency Trade-offs in Self-Checking Memory Design
O. Kebichi, M. Nicolaidis, and Y. Zorian

Self-Checking Architectures for Fast Hartley Transform

Built-in Intermediate Voltage Testing for CMOS
J.-J. Tang, K.-J. Lee, and B.-D. Liu