Session 6C: Test Generation and Testability

Moderators: W. Geisselhardt, University of Duisburg, Germany and P. Prinetto, Politecnico di Torino, Italy

The first paper addresses the problem of test quality obtained by using unbiased testing. The second one proposes a new approach to compute testability of a VLSI circuit in a hierarchical design environment. The last contribution deals with delay fault test pattern generation for sequential circuits.

Enhanced Testing Performance Via Unbiased Test Sets
L.-C. Wang, M.R. Mercer, and T.W. Williams

A Testability Measure for Hierarchical Design Environments
M.H.C. Lee and D.L. Tao

Gate Delay Fault Test Generation for Non-Scan Circuits