Session 5B: Code Generation
Moderators: J. van Meerbergen, Philips Research, The Netherlands and G. Goossens, IMEC, Belgium

Code generation for embedded instruction-set processors is a topic of growing importance, especially in the field of DSP. In this Session new techniques and models are presented for code generation. The first and third paper focus on scheduling issues. The second paper discusses instruction extraction from processor netlists.

A Unified Scheduling Model for High-Level Synthesis and Code Generation
A. Kifli, G. Goossens, and H. De Man

A BDD-Based Frontend for Retargetable Compilers
R. Leupers and P. Marwedel

Efficient Code Generation for In-House DSP-Cores