Session 5A: Digital and System Simulation

Moderators: F.-J. Rammig, Universitat GH Paderborn and J. Mermet, Artemis, France

In the first paper mixed signal simulation capabilities of VHDL for system-on-chip applications are demonstrated. The second contribution presents a new concept to implement event monitors. The third paper discusses novel delay-models for sea-wire arrays

Mixed-Signal Modeling in VHDL for System-On-Chip Applications
F. Pichon, S. Blanc, and B. Candaele

Run-Time Consistency Checking in Discrete Simulation Models

Delay Models for the Sea-of-Wires Array Synthesis System
I.-Y. Chen, G.L. Chen, and S.-Y. Kuo