Session 4A: High Speed Telecom Design
Moderators: J.L Conesa, Telefonica I+D, Spain and M. Diaz Nava, SGS Thomson Microelectronics, France

This Session discusses new architectures and design techniques for advance high speed telecom systems. ECL and mixed ECL/CMOS designs will be presented and discussed.

Input and Output Processor for an ATM High Speed Switch (2.5 gb/s): The CMC
P. Plaza, J.C. Diaz, F. Calvo, L. Merayo, M. Zamboni, P. Scarfone, and M. Barbini

Post-Layout Optimization of Power and Timing for ECL LSIs
A. Onozawa, K. Kawai, and H. Kitazawa

A 622/155 Mbps ATM Line Terminator Mono-Chip
M. Diaz Nava, D. Belot, P. Delerue, and J. Bulone