Session 3C: Sequential Logic Synthesis
Moderators: G. De Micheli, Stanford University, USA and G. Saucier, INPG/CSI, France

Three papers are presented in this Session on modeling and synthesis of sequential circuits. The first paper describes a new model for the representation and optimization of hierarchical synchronous circuits. The second paper addresses the initialization problem in retiming. The third paper presents a new FGM encoding algorithm that avoids sequential false paths.

Modeling and Optimization of Hierarchical Synchronous Circuits
B. Lin, G.G. de Jong and T. Kolks

Improving Initialization Through Reversed Retiming
L. Stok, I. Spillinger, and G. Even

Elimination of Multi-Cycle False Paths by State Encoding
Z. Hasan and M.J. Ciesielski