Test Preparation Methodology for High Coverage of Physical Defects in CMOS Digital ICs

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Abstract
The constant increase of IC circuit complexity and quality requirements make high quality testing a difficult challenge. In this work, a methodology for test preparation leading to high physical defect coverage is proposed. Two new software tools are presented, that implement the proposed methodology, tabloid and iceTgen. From the gate level schematics, a heuristic is proposed to generate a list of pseudo-realistic faults that, when used as target faults for test pattern generation, lead to high coverage of physical defects with a shorter test sequence than the one generated using realistic faults extracted from the layout.

Introduction
The purpose of this work is to present a methodology for high quality test preparation, at gate level, leading to high values of the defect (or realistic faults) coverage. Failure mechanisms in present day CMOS process lines, using positive photoresist, are dominated by extra material failures. Therefore, bridging faults (BRI) are assumed in this work.

Test Preparation Methodology
Test pattern generation and fault simulation at transistor level are prohibitive for large circuits. Hence, higher levels of abstraction are required to reduce the computational costs of test preparation. Using a gate-level circuit description, we need fault models that, accurately, characterize the logic behavior of the circuit in the presence of each likely physical defect. tabloid is a new software tool that starts from transistor level information, and performs logic extraction, identifying logic elements, their connectivity and functionality. To describe, at logic level, the behavior of the circuit in the presence of a BRI fault, tabloid creates a truth table describing the logic function for the local, damaged sub-circuit in the presence of the fault. This truth table can contain 'Xs' if, as a consequence of the BRI, the voltage in the nodes involved, is within the uncertainty range. This uncertainty range results from different threshold voltages associated with the logic elements inputs.

The program iceTgen is a new ATPG tool for realistic faults that takes into account the faulty circuit local behavior (provided by tabloid). Test vectors are generated for voltage detection using the defined values of local true tables. If the fault is not detected, the 'Xs' are used with the associated four possibilities (each node can dominate with 1 or 0). The test vectors generated this way don't contribute to firm detection. However, they contribute to soft detection. The faults not detected by firm detection are also target faults for current detection, also carried out by the tool. The iceTgen can also perform test pattern generation using as target faults pseudo-realistic faults. These faults are obtained from the gate description of the circuit using the following criteria:

- add to the pseudo-realistic fault list all possible BRIs between all nodes of each logic element;
- add to the pseudo-realistic fault list the BRIs between nodes which are more probable to share the same routing channel. Such probability is translated in terms of the vicinity of logic elements in the schematics;
- do not include as pseudo-realistic faults, those associated with nodes with high fanout values. Our study indicates that LSA vectors detects well realistic faults associated to nodes with fanout higher than 3.

Two approaches are possible with the new tools: a Bottom-up Approach, starting from the IC layout (the ATPG uses realistic faults as target faults), and a Top-Down Approach, for which a traditional stuck-at based ATPG is complemented using the pseudo-realistic faults as target faults for voltage and current test.

In the presentation, benchmark circuits are used to demonstrate the usefulness of the methodology, and the high defects coverage thus achieved.

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