High Speed Communications Links for Asics

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ASIC integration and speeds have risen rapidly in the past couple of years to the point now where 50 to 100 MHz clock rates and hundreds of thousands of used gates are commonplace. These performance and integration levels place huge demands on chip-to-chip data transfer and packaging, with communications rates of up to 1 Gbit/sec being required. This poster compares some of the traditional I/O standards available to an ASIC designer such as TTL, CMOS with some of the more recent advances such as PECL, GTL, and LVDS.

Design considerations and limitations of these modern schemes are explored. In particular, the operation of LSI Logic’s implementation of LVDS is presented along results from 0.5 micron Silicon.

Other considerations such as the accurate modelling of the operating environment of very fast ASIC communications links are reviewed, including package parasitics and other off silicon effects. While it is difficult to determine the ultimate limits for communications outside of a package it will be shown through simulation and measurement that internal silicon clock frequencies in excess of 1GHz are realizable today using a 0.5 micron CMOS process. However, the biggest problem that is facing the high speed interface designer today is in obtaining a realistic model for cables and packages. A full electrical understanding and characterization of the total system is the only solution to achieving at the system level the performance now achievable on the silicon.