Session 40
Timing Analysis and Optimization

Chair: Ibrahim N. Hajj
Organizers: K. Sakallah, S. Malik

This session covers innovations in timing analysis and optimization. The papers cover diverse issues such as gate and interconnect sizing for performance optimization, consideration of statistical issues in gate delay modeling, incremental timing analysis of latch-based systems and abstraction of clocks to speed up logic simulation.

40.1 Simultaneous Gate and Interconnect Sizing for Circuit-Level Delay Optimization
   Noel Menezes, Satyamurthy Pullela, Lawrence T. Pileggi

40.2 An Algorithm for Incremental Timing Analysis
   Jin-fuw Lee, Donald T. Tang

40.3 An Assigned Probability Technique to Derive Realistic Worst-Case Timing Models of Digital Standard Cells
   Alessandro Dal Fabbro, Bruno Franzini, Luigi Croce, Carlo Guardiani

40.4 Automatic Clock Abstraction from Sequential Circuits
   Samir Jain, Randal E. Bryant, Alok Jain