Session 39
Complexity Measures for VHDL

Chair: Reinaldo A. Bergamaschi
Organizers: A. Domic, R. McGeer

This session examines the complexity of VHDL programs. The first paper, a tutorial, relates VHDL descriptions to logic circuits. The second and third papers introduce information-theoretic and software engineering metrics to VHDL programs.

39.1 Tutorial: Productivity Issues in High-Level Design: Are Tools Solving the Real Problems?
   Reinaldo A. Bergamaschi

39.2 Information Models of VHDL
   Cristian A. Giumale, Hilary J. Kahn

39.3 Measures of Syntactic Complexity for Modeling Behavioral VHDL
   Neal S. Stollon, John D. Provence