Routing methods for both intra- and inter-FPGAs are proposed. The first paper addresses the interconnection problem for a crossbar-connected multiple-FPGA system. The next two papers present performance-driven routing based on a rip up-and-reroute approach and a Steiner-tree construction, respectively. The fourth paper tries an interesting combination of different heuristics during different stages of routing. The session concludes with a presentation on important issues in FPGA routing from an industrial point of view.

33.1 On Optimal Board-Level Routing for FPGA-Based Logic Emulation
    Wai-Kei Mak, D.F. Wong

33.2 A Performance and Routability Driven Router for FPGAs Considering Path Delays
    Yuh-Sheng Lee, Allen C.-H. Wu

33.3 New Performance-Driven FPGA Routing Algorithms
    Michael J. Alexander, Gabriel Robins

33.4 Orthogonal Greedy Coupling - A New Optimization Approach to 2-D FPGA Routing
    Yu-Liang Wu, Malgorzata Marek-Sadowska

33.5 Effects of FPGA Architecture on FPGA Routing
    Stephen Trimberger