Session 32
Formal Verification of Arithmetic Circuits

Chair: Gary D. Hachtel
Organizers: K. Keutzer, F. Somenzi

The verification of arithmetic circuits has proved very troublesome to BDD-based formal verification approaches. In this session, three new approaches to this fundamental problem demonstrate their promising results.

32.1 Verification of Arithmetic Circuits with Binary Moment Diagrams*
   Randal E. Bryant, Yirng-An Chen

32.2 Residue BDD and Its Application to the Verification of Arithmetic Circuits
   Shinji Kimura

32.3 Equivalence Checking of Datapaths Based on Canonical Arithmetic Expressions
   Zheng Zhou, Wayne Burleson

*Best Paper Award candidate