Session 24
Learning and Counterexamples
in Formal Verification

Chair: Carl Pixley
Organizers: F. Somenzi, K. Keutzer

Practical application of formal verification requires the ability to provide feedback to the user and the ability to overcome capacity limitations of straightforward BDD-based methods. This session addresses these topics, presenting applications of learning techniques to ATPG-based verification, and discussing the generation of good counterexamples when verification uncovers a bug in a design.

24.1 Efficient OBDD-Based Boolean Manipulation in CAD beyond Current Limits
   Jochen Bern, Christoph Meinel, Anna Slobodová

24.2 Novel Verification Framework Combining Structural and OBDD Methods in a Synthesis Environment
   Subodh M. Reddy, Wolfgang Kunz, Dhiraj K. Pradhan

24.3 Advanced Verification Techniques Based on Learning
   Jawahar Jain, Rajarshi Mukherjee, Masahiro Fujita

24.4 Efficient Generation of Counterexamples and Witnesses in Symbolic Model Checking
   E. M. Clarke, O. Grumberg, K. L. McMillan, X. Zhao