Session 21
CAD for Interconnect

Chair: Andrzej J. Strojwas
Organizers: A. Strojwas, J. White

The first three papers in this session address the delays in interconnect/transmission lines. The first paper proposes an approach to constraint generation for interconnect synthesis, the next proposes an upper bound for the delay, and the third derives approximations to delays in RC lines terminated with a capacitive load. The next paper proposes a reduced-order modeling approach for coupling inductance computations. The final paper presents an approach for performance-driven routing in high speed MCMs and PCBs.

21.1 Transmission Line Synthesis
Byron Krauter, Rohini Gupta, John Willis, Lawrence T. Pileggi

21.2 The Elmore Delay as a Bound for RC Trees with Generalized Input Signals
Rohini Gupta, Byron Krauter, Bogdan Tutuianu, John Willis, Lawrence T. Pileggi

21.3 Delay Analysis of the Distributed RC Line
Vasant B. Rao

21.4 Efficient Reduced-Order Modeling of Frequency-Dependent Coupling Inductances Associated with 3-D Interconnect Structures
L. Miguel Silveira, Matton Kamon, Jacob White

21.5 Performance Driven Global Routing and Wiring Rule Generation for High Speed PCBs and MCMs
Sharad Mehrotra, Paul Franzon, Michael Steer