Session 18
Advanced Methods in Practice

Chair: Don Stark
Organizers: D. Stark, N. Weste

With rapidly evolving design techniques, there is often a considerable gap between theory and practice. The emphasis in this session is on emerging CAD techniques to close this gap. The first paper describes a functional test strategy for an advanced microprocessor family. The second paper describes a framework for creating efficiently synthesizable behavioral descriptions. The third paper describes how formal synthesis can be applied to ASIC design. The final paper shows the application of formal methods to hardware model verification.

18.1 Test Program Generation for Functional Verification of PowerPC Processors in IBM*
     Aharon Aharon, Dave Goodman, Moshe Levinger, Yossi Lichtenstein, Yossi Malka, Charlotte Metzger, Moshe Molcho, Gil Shurek

18.2 Behavioral Synthesis Methodology for HDL-Based Specification and Validation*
     D. Knapp, T. Ly, D. MacMillen, R. Miller

18.3 Design-Flow and Synthesis for ASICs: A Case Study
     Massimo Bombana, Patrizia Cavalloro, Salvatore Coniglio, Roger B. Hughes, Gerry Musgrave, Giuseppe Zaza

18.4 Model Checking in Industrial Hardware Design
     Jörg Bormann, Jörg Lohse, Michael Payer, Gerd Venzl

*Best Paper Award candidate