Session 17
Extraction and Module Generation

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The first two papers describe methods for automatic module layout generation of RAM blocks and leaf cells. Practical considerations include simulation and transistor sizing. The third paper deals with the speed-memory trade-off for extracting parasitic resistance from layout. This is an important parameter for high-performance design in the deep submicron era.

17.1 The Aurora RAM Compiler
Ajay Chandna, C. David Kibler, Richard B. Brown, Mark Roberts, Karem A. Sakallah

17.2 Automatic Layout Synthesis of Leaf Cells
Sanjay Rekhi, J. Donald Trotter, Daniel H. Linder

17.3 Delayed Frontal Solution for Finite-Element Based Resistance Extraction
N.P. van der Meijs, A.J. van Genderen