Innovative design techniques are rapidly finding use in real-world industrial designs. This session includes VHDL simulation of Siemens’ EWSD-System’s processor, digital receiver design using generated VHDL generated from Data Flow Graphs, and Logic Verification for PowerPC.

14.1 Concurrent Design Methodology and Configuration Management of the Siemens EWSD - CCS7E Processor System Simulation
   Thomas W. Albrecht

14.2 Digital Receiver Design Using VHDL Generation from Data Flow Graphs*
   Peter Zepter, Thorsten Grötker, Heinrich Meyr

14.3 Logic Verification Methodology for PowerPC™ Microprocessors
   Charles H. Malley, Max Dieudonné

*Best Paper Award candidate