The opening paper of this session gives a characterization of the correspondence between spectral partitioning and graph partitioning; a new heuristic for multi-way partitioning is also given. Two papers then address multi-way partitioning for minimum delay and area, and the use of replication cuts for improvement of delay and cycle time. In the fourth paper, pin-to-pin delay analysis improves the well-known Timberwolf layout package. The concluding paper offers a measure of the scaling behavior of layout heuristics, and suggests that there is room for improvement over current leading methods.

13.1 Spectral Partitioning: The More Eigenvectors, the Better*

Charles J. Alpert, So-Zen Yao

13.2 Multi-way Partitioning for Minimum Delay for Look-Up Table Based FPGAs

Prashant Sawkar, Donald Thomas

13.3 Performance-Driven Partitioning Using a Replication Graph Approach

Lung-Tien Liu, Ming-Ter Kuo, Chung-Kuan Cheng, Te C. Hu

13.4 Timing Driven Placement for Large Standard Cell Circuits

William Swartz, Carl Sechen

13.5 Quantified Suboptimality of VLSI Layout Heuristics

Lars W. Hagen, Dennis J.-H. Huang, Andrew B. Kahng

*Best Paper Award candidate