Session 9
Discrete-Event Simulation

Chair: Peter M. Maurer
Organizers: M. Bailey, R. McGeer

These papers relate to discrete-event simulation. The tutorial surveys the current state of parallel discrete-event simulation. The second paper is a new algorithm for parallel discrete-event simulation for VHDL. The final paper uses compiler optimization techniques to increase the performance of event-driven simulation.

9.1 Tutorial: Parallel Logic Simulation of VLSI Systems
Roger D. Chamberlain

9.2 Asynchronous, Distributed Event Driven Simulation Algorithm for Execution of VHDL on Parallel Processors
Peter A. Walker, Sumit Ghosh

9.3 A General Method for Compiling Event-Driven Simulations
Robert S. French, Monica S. Lam, Jeremy R. Levitt, Kunle Olukotun