Session 8
Delay Test and Diagnosis

Chair: Peter C. Maxwell
Organizers: J. Patel, J. Rajski

Papers in this session explore synthesis techniques to reduce the number of paths to be tested, other algorithmic approaches towards considering fewer paths and diagnosis of sequential circuits.

8.1 Fast Identification of Robust Dependent Path Delay Faults
   U. Sparmann, D. Luxenburger, K.-T. Cheng, S.M. Reddy

8.2 On Synthesis-for-Testability of Combinational Logic Circuits
   Irith Pomeranz, Sudhakar M. Reddy

8.3 Rapid Diagnostic Fault Simulation of Stuck-at Faults in Sequential Circuits Using Compact Lists
   Srikanth Venkataraman, Ismed Hartanto, W. Kent Fuchs, Elizabeth M. Rudnick, Sreejit Chakravarty, Janak H. Patel