Session 4
Technology and Layout Dependent Synthesis

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Organizers: M. Pedram, G. Saucier

This session focuses on the impact of the target technology and layout on logic synthesis. The first paper extends Boolean matching to incompletely specified Boolean functions. The next three address single and multiple output function decomposition for LUT-based devices. The last paper combines synthesis with layout optimization.

4.1 Boolean Matching for Incompletely Specified Functions*
   *Kuo-Hua Wang, TingTing Hwang

4.2 Functional Multiple-Output Decomposition: Theory and an Implicit Algorithm*
   *Bernd Wurth, Klaus Eckl, Kurt Antreich

4.3 A Method for Finding Good Ashenhurst Decompositions and Its Application to FPGA Synthesis
   *Ted Stanion, Carl Sechen

4.4 Lambda Set Selection in Roth-Karp Decomposition for LUT-Based FPGA Technology Mapping
   *Wen-Zen Shen, Juinn-Dar Huang, Shih-Min Chao

4.5 Minimizing the Routing Cost during Logic Extraction
   *Hirendu Vaishnav, Massoud Pedram

*Best Paper Award candidate