Session A-5B
Logic Synthesis and Optimization (1)

Chair: Bernd Becker
Co-Chair: Tetsuya Fujimoto

A-5B.1 Communication Based FPGA Synthesis for Multi-Output Boolean Functions
Christoph Scholl, Paul Molitor

A-5B.2 Optimum PLA Folding through Boolean Satisfiability
J.M. Quintana, M.J. Avedillo, M.P. Parra, J.L. Huertas

A-5B.3 Technology Mapping for FPGAs with Complex Block Architectures by Fuzzy Logic Technique
Jun-Yong Lee, Eugene Shragowitz

A-5B.4 Logic Rectification and Synthesis for Engineering Change
Chih-Chang Lin, David Ihsin Cheng, Kuang-Chien Chen, Malgorzata Marek-Sadowska