[Invited Tutorial]

EDIF Version 350/400 and Information Modelling

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The design and implementation of the EDIF family of standards is based on the use of the specification technique called information modelling. The goal of information modelling is to provide the standards development process with a methodology that will ensure, as far as is possible, that the contents of the standard are correct, consistent and clearly defined.

To achieve this goal, it is essential to separate the semantics of the information carried by a given standard, such as EDIF, and the syntax used to support tools based on the standard. In EDIF, there is a very clear separation here: the information model alone defines the semantics of the standard using a simple but powerful modelling method. The syntax of the format is defined separately as a formal BNF and is supported by a more traditional Language Reference Manual which includes practical examples.

In this tutorial, the presentation will also be separated. In the first part, the concepts underlying the technique of information modelling will be explained. The information modelling method used will be EXPRESS [ISO 10303.11], the ISO standard modelling language which has been used in the EDIF organization for over 5 years. EXPRESS is based on a combination of specification and language paradigms, but owes a great deal to the object-oriented tradition.

The first part of the talk will address the high level concepts and goals of information modelling. It will look at the basic mechanisms EXPRESS provides for capturing the essential objects and attributes of a domain and how those objects are inter-related. Above all, it will concentrate on how constraints are used to ensure that the information model is explicit and unambiguous.

The second part of the presentation will focus on the content of EDIF Version 3 5 0 and EDIF Version 4 0 0. The general architecture of the new EDIF standard will be introduced and used to show how extensions of EDIF into the new domains of PCB and MCM are supported. The solutions adopted in EDIF to ensure a representation with minimal context dependency and hence, it is hoped, minimal ambiguity will be highlighted.

EDIF Version 3 5 0 enhances the EDIF standard beyond the connectivity (netlist) and schematics capability in EDIF Version 3 0 0 into the PCB domain. It includes the representation of a PCB as a layered product with support for both bare boards and assembled boards. EDIF Version 3 5 0 supports functional and component netlists, parts libraries and components, allocation, gate and pin swapping, layout details such as padstacks and footprints, some materials information and manufacturing data. How this information is supported will be outlined by reference to the relevant parts of the EDIF Version 3 5 0 information model.

The presentation will conclude by looking at the further enhancements that are being made to EDIF Version 3 5 0 to produce EDIF Version 4 0 0. The talk will concentrate on aspects of the multi-chip module (MCM) representation where EDIF now provides support for a range of MCM technologies and both the chip-first and the chip-last bare die attachment methods. In addition, there will be a brief look at the work being included for the support of PCB drawings (assembly drawings and drill drawings) and the handling of technology-related rules for both PCBs and MCMs.