

# Pin Assignment and Routing on a Single-Layer Pin Grid Array

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PGA routing has the freedom of routing any pin to any pad. We proposed an algorithm (EVENPGA) that generates a monotonic topological routing. The routing has no detours and is uniformly distributed optimally. The wire length is also the shortest possible under the taxicab wiring metric. If the topological routing is routable, the maximum density of critical cuts along a ring is the minimum possible. Once the topological routing is done, physical layout can easily be obtained using Surf, a rubberband-based routing system.

## I. INTRODUCTION

A single-layer pin grid array (PGA) package contains a chip cavity with a single row of wire-bond pads and a rectangular array of pins (Fig. 1). At present, most PGA routing is done manually. As the I/O pin count increases, routing a PGA becomes a non-trivial task. In this paper we consider the relationship of pin assignment and routing of a single-layer PGA package. This routing problem is different from general area routing in several ways:

- There is no netlist. Each bond pad needs to be routed to one and only one pin. All pins are equivalent.
- The routing pattern is highly symmetric. The pins are on a grid with uniform pitch. The whole package is symmetrical.
- The wires may be routed in all angles.

This paper is the first to consider pin assignment in a package routing. The algorithms proposed in this paper guarantee a planar routing with the most uniform distribution of wires and shortest wire length in the taxicab wiring metric[1]. Previous work by Ying and Gu[2] and Tsai and Chen[3] require an input netlist. Both approaches use the technique of iterative improvement. Our algorithm creates a topological routing directly and with optimal wire distribution. The only previous work on package routing that considers pin assignment is by Darnauer and Dai[4].

We start with the proof of an important theorem that relates a monotonic pin assignment to a monotonic topological routing. This theorem is the cornerstone of the routing algorithm. Next we present the routing algorithm

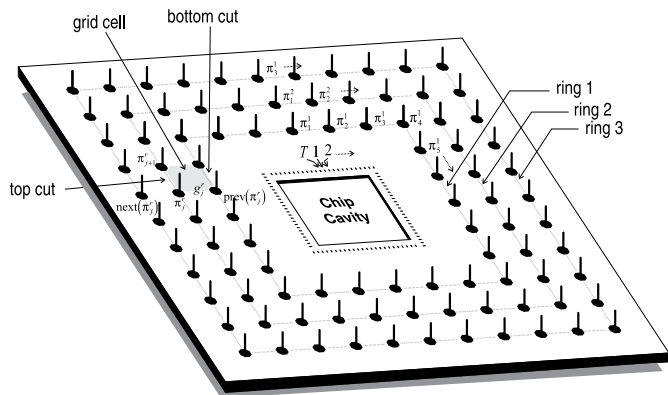


Fig. 1. A conceptual single-layer PGA package.

which generates a monotonic topological routing. The rest of the paper analyzed the properties of the topological routing created by the routing algorithm. The two important results are uniform distribution of wiring and shortest wire length.

The transformation of topological routing to detailed routing including design-rule check and final geometry transformation is done by Surf[5, 6, 7, 8, 9].

## II. MONOTONIC PIN ASSIGNMENT

Assume a PGA package has  $T$  pads  $X = \{1, 2, \dots, T\}$  arranged in a clockwise manner starting at the center of an arbitrary side of the chip cavity (Fig. 1). The package also has  $R$  pin rings  $\Pi = \cup_{r=1}^R \Pi^r$ , where each ring  $r$  consists of  $P_r$  pins  $\Pi^r = \{\pi_1^r, \pi_2^r, \dots, \pi_{P_r}^r\}$ . Since the pins are arranged in rings, all arithmetic involving the subscript of a pin should be modulo  $P_r$ . To simplify the mathematics, we assume that the number of pins of innermost ring, ring 1, is divisible by 8. If the number of pins in ring 1 is  $8N$ , we have  $T = 4R(2N + R - 1)$  and  $P_r = 8(N + R - 1)$ .

The problem of routing a single-layer PGA (1LPGA) can be defined as follows:

**Problem 1 (1LPGA)** *The single-layer pin grid array routing (1LPGA) problem is to create detailed routing given the set of pins  $\Pi$  and the set of pads  $X$  in such*

a way that there is no routing allowed in the chip cavity and each pad is to be connected to one and only one pin.

1LPGA assumes  $|\Pi| = |X|$ . 1LPGA can be solved by finding a pin assignment and then create a routing.

**Definition 1** A pin assignment is a one-to-one and onto mapping  $\Phi : \Pi \rightarrow X$ .

**Definition 2** A monotonic topological routing (MTR) is a topological routing such that all wires  $w = (\pi_j^r, p)$  satisfy the following conditions:

1. **Detour Condition** intersect at most one cut  $(\pi_k^s, \pi_{k+1}^s)$  for some  $k$  in all the rings  $s$ , and
2. **Chip Cavity Condition** does not intersect cuts  $(q, q+1)$  for all  $q \in X$ , and
3. **Shortest Path Condition** is shortest between pad  $p$  and the cut on ring 1 that intersects  $w$ , i.e. the cut  $(\pi_k^1, \pi_{k+1}^1)$  where  $\Phi(\pi_k^1) < p < \Phi(\pi_{k+1}^1)$ . If  $w$  is a connection between  $p$  and a pin in ring 1, then  $w$  is the shortest path between the pad and the pin.

MTR is usually the desired routing because the wire length is the shortest possible. It turns out that each MTR has a unique *monotonic pin assignment (MPA)*.

**Definition 3** A monotonic pin assignment (MPA) is a pin assignment such that for all  $r$ ,  $\Phi(\pi_i^r) > \Phi(\pi_j^r)$  if and only if  $i > j$ .

**Lemma 1** Given a monotonic pin assignment, a monotonic topological routing exists.

**Proof:** We construct the routing as follows: Starting with ring 1, we fanout the wires from the pad frame to the ring using the shortest path possible. The wires are not allowed to enter the chip cavity. If a pad is assigned to a pin in ring 1, then make the connection. Otherwise, place the wire (say from pad  $p$ ) between the cut of adjacent pins  $\pi_i^1$  and  $\pi_{i+1}^1$  where  $\Phi(\pi_i^1) < p < \Phi(\pi_{i+1}^1)$  or, if  $p > \Phi(\pi_i^1)$  for all  $i$ , choose the cut  $(\pi_1^1, \pi_{P_r}^1)$ . Arrange the wire order in each cut between pairs of pins in ring 1 such that, if the ordering is  $(\pi_i^1, w_1, w_2, \dots, w_n, \pi_{i+1}^1)$ , then  $\Phi(\text{pinof}(w_i)) < \Phi(\text{pinof}(w_{i+1}))$ . Repeat the operation on ring 2, 3,  $\dots$ ,  $R$ .

It is obvious that each wire  $w = (\pi_i^r, p)$  intersects rings 1,  $\dots$ ,  $r-1$  only once. So there is no detour. Consider the whole ring  $r$  as a cut. The order of wires and pins on the cut is in the same order as the wires by construction. Therefore no wires need to cross each other so the construction will not create wires that enter the chip cavity.

Finally, the shortest path from pad to ring 1 for all wires guarantees the shortest path condition.  $\square$

**Lemma 2** Given a monotonic pin assignment, there is a unique monotonic topological routing.

### Algorithm 1 (EVENPGA)

Algorithm EVENPGA(Set of Pins  $\Pi$ , Ordered set of pads  $X$ )

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For rings  $r \leftarrow 1$  to  $R$ 
  Stepsize  $k \leftarrow \lfloor |X|/P_r \rfloor$ 
  Remainder  $q \leftarrow |X| - kP_r$ 
  Pin number  $j \leftarrow 1$ 
  For pads  $i \leftarrow 1$  to  $|X|/8$ 
    ASSIGN8( $X[i], j, r$ )
     $j \leftarrow j + 1$ 
    If  $i \leq (q/8)(k + 1)$ 
      Then  $i \leftarrow i + k + 1$ 
    Else  $i \leftarrow i + k$ 
  Endfor
  Remove all assigned pads from  $X$ 
Endfor

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Subroutine ASSIGN8( $i, j, r$ )
  Assign pad  $i$  to pin  $\pi_j^r$  (Sector 1)
  Assign pad  $|X|/4 - i + 1$  to pin  $\pi_{P_r/4 - j + 1}^r$  (Sector 2)
  Assign pad  $|X|/4 + i - 1$  to pin  $\pi_{P_r/4 + j - 1}^r$  (Sector 3)
  Assign pad  $|X|/2 - i + 1$  to pin  $\pi_{P_r/2 - j + 1}^r$  (Sector 4)
  Assign pad  $|X|/2 + i - 1$  to pin  $\pi_{P_r/2 + j - 1}^r$  (Sector 5)
  Assign pad  $3|X|/4 - i + 1$  to pin  $\pi_{3P_r/4 - j + 1}^r$  (Sector 6)
  Assign pad  $3|X|/4 + i - 1$  to pin  $\pi_{3P_r/4 + j - 1}^r$  (Sector 7)
  Assign pad  $|X| - i + 1$  to pin  $\pi_{P_r - j + 1}^r$  (Sector 8)

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Fig. 2. Algorithm EVENPGA.

**Proof:** By contradiction. Suppose there are two MTRs for a given MPA. Then there exists a pin  $\pi_i^r$  such that there are two possible topological routing  $w_1$  and  $w_2$  for the same assignment  $(\pi_i^r, p)$ . Since they are topologically different and the routing is an MTR, there exist two pins  $\pi_j^s$  and  $\pi_k^t$  where  $s, t < r$ , such that exactly one of the wires crosses the cut  $c = (\pi_j^s, \pi_k^t)$ . Assume without loss of generality that  $w_1$  crosses the cut and  $\Phi(\pi_j^s) < \Phi(\pi_k^t)$ . Since  $w_1$  crosses  $c$ , we have  $\Phi(\pi_j^s) < p < \Phi(\pi_k^t)$ . Also, since  $w_2$  does not cross  $c$ , we have either  $p < \Phi(\pi_j^s)$  or  $p > \Phi(\pi_k^t)$ . This is a contradiction. Hence it is impossible to have two topological routing for an MPA.  $\square$

Combining Lemma 1 and Lemma 2, we have:

**Theorem 1 (Existence and Uniqueness)** *There exists a unique monotonic topological routing for any given monotonic pin assignment.*

### III. CREATING AN MTR

Since by Theorem 1 an MPA has a unique MTR, all we need is an algorithm that creates an MPA.

EVENPGA (Fig. 2) takes advantage of the symmetric geometry of the package and divides it into eight sectors. Fig. 3 shows the direction of assignment in each sector and the dividing lines.

**Algorithm 2 (MAKEMTR)**

Algorithm MAKEMTR( $\Phi, X, \Pi$ )

For  $r \leftarrow 1$  to  $R$   
 For  $i \leftarrow 1$  to  $P_r$   
 Route  $\pi_i^r$  to  $\Phi(\pi_i^r)$

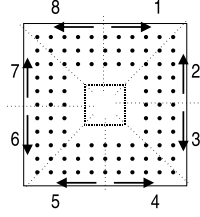


Fig. 3. MAKEMTR and the assignment directions in each sector.

Since each pad is visited once, EVENPGA runs in order  $O(|X|)$ . The storage complexity is the size of the output, i.e.  $O(|\Phi|) = O(|X|)$ .

Also note that all arithmetics are integer. All divisions have no remainders except the line marked (\*). We can observe that the number of assigned pins is  $P_r$  in each iteration and both  $|X|$  and  $q$  are divisible by 8.

It is straightforward to verify that EVENPGA creates an MPA. After the assignment, we can generate the topological routing using the simple algorithm MAKEMTR (Fig. 3).

The routing from  $\pi_i^r$  to  $\Phi(\pi_i^r)$  is created by the shortest-path algorithm described by Dai, Dayan and Staepelaere[6].

MAKEMTR is correct because the wire length is the shortest possible for all wires. Section V analyzed the wire lengths of the routing created by EVENPGA. The time complexity of MAKEMTR is  $O(|X|S)$  where  $S$  is the time complexity of routing one wire.

IV. UNIFORM WIRING DISTRIBUTION

An important property of EVENPGA is that it distributes the wires as uniformly as possible around the rings. The pin assignment ordered the wiring in such a way that no crossing is necessary. This is a major advancement over previously proposed algorithms[3, 2].

To simplify the mathematics, we assume that the pin pitch is 1 unit distance. Let the expression  $\text{next}(\pi_i^r)$  denote the pin on ring  $r + 1$  that is closest to  $\pi_i^r$ . Note that  $\text{next}()$  is undefined for a corner pin. Similarly,  $\text{prev}(\pi_i^r)$  denote the pin on ring  $r - 1$  that is closest to  $\pi_i^r$ . We define a *grid cell*  $g_i^r$  to be the area bounded by the pins  $\pi_i^r, \pi_{i+1}^r, \text{prev}(\pi_i^r)$  and  $\text{prev}(\pi_{i+1}^r)$ .  $\pi_i^r$  cannot be a corner pin. If  $\pi_{i+1}^r$  is a corner pin, then the cell is defined by the area bounded by  $\pi_i^r, \pi_{i+1}^r, \pi_{i+2}^r$  and  $\text{prev}(\pi_i^r)$ . Intuitively,  $\pi_i^r$  is at the upper left corner of  $g_i^r$ . We define the *bottom cut* of a cell  $g_i^r$  to be the cut  $(\text{prev}(\pi_i^r), \text{prev}(\pi_{i+1}^r))$ , the *top cut* to be  $(\pi_i^r, \pi_{i+1}^r)$ , the *left side cut* to be  $(\pi_i^r, \text{prev}(\pi_i^r))$  and the *right side cut* to be  $(\pi_{i+1}^r, \text{prev}(\pi_{i+1}^r))$ . Fig. 1 shows a pin  $\pi_i^r, \text{next}(\pi_i^r), \text{prev}(\pi_i^r)$  and the grid cell  $g_i^r$ .

Now we proceed to prove that EVENPGA produces a uniformly distributed topological routing. The follow-

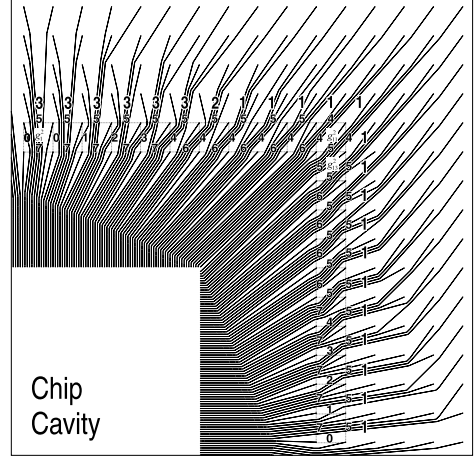


Fig. 4. Top right quadrant of a PGA package.

ing lemma states that the wires are uniformly distributed among the cuts in all the rings.

**Lemma 3** For all  $r = 1, \dots, R$ ,

$$\max_{\forall i} (F(\pi_i^r, \pi_{i+1}^r)) - \min_{\forall i} (F(\pi_i^r, \pi_{i+1}^r)) \leq 1.$$

$F(\pi_i^r, \pi_j^r)$  is the flow of the cut  $(\pi_i^r, \pi_j^r)$ , i.e. the number of wires intersecting the cut.

**Proof:** By induction on  $r$ . For ring 1, in each iteration of  $i$ , it is incremented by either  $k$  or  $k + 1$ . Hence the number of wires between any two adjacent pin in ring 1 is either  $k - 1$  or  $k$ . Therefore

$$\max_{\forall i} (F(\pi_i^r, \pi_{i+1}^r)) - \min_{\forall i} (F(\pi_i^r, \pi_{i+1}^r)) \leq k - (k - 1) = 1.$$

Now assume that it is true for rings  $1, 2, \dots, r$ . Consider ring  $r + 1$ . Since the pads assigned to the first  $r$  rings are removed from the set  $X$ , this is exactly the problem instance  $(\Pi', X')$  where  $\Pi' = \cup_{i=r+1}^R \Pi^i$  and  $X' = X -$  all assigned pads. By a similar argument as ring 1, it is true for ring  $r + 1$ .  $\square$

Lemma 3 show that the density along a ring is even. Now we investigate the side flows. We start with a lemma that relates the step sizes of adjacent rings.

**Lemma 4** Let  $k_r$  and  $k_{r+1}$  are the values of  $k$  in iteration  $r$  and  $r + 1$  respectively. If  $R < \sigma$  then  $0 < k_r - k_{r+1} < 3$  where  $\sigma = 1/2 - N + \sqrt{3N^2 + 3N + 1}/4$ .

**Proof:** The result can be derived easily by recognizing that at iteration  $r$ ,  $|X| = T - 4(r - 1)(N + r - 2)$  and  $R \geq r$ .  $\square$

Since  $\sigma > N/2$  and in most packages  $R$  is far less than  $N$ , this requirement is not a strong constraint. From now on we will assume that  $R$  always satisfy this requirement.

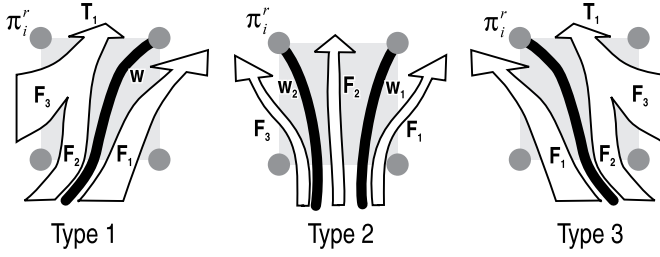


Fig. 5. The flows of a grid cell.

We will now derive a relationship between the step sizes of adjacent rings. The following lemma states that the maximum difference is at most 2. This is because of the relative magnitudes of the remainder  $q$ .

**Lemma 5** *Let  $T_i^r$  be the flow of the top cut of a cell  $g_i^r$  and  $B_i^r$  be the flow of the bottom cut of the same cell. Then  $1 \leq B_i^r - T_i^r \leq 2$  if  $R < \sigma$ .*

**Proof:** Since  $k_r - 1 \leq T_i^r \leq k_r$  and  $k_{r-1} - 1 \leq B_i^r \leq k_{r-1}$ , we have  $B_i^r - T_i^r \leq k_{r-1} - k_r + 1$ . By Lemma 4, either  $k_{r-1} - k_r = 1$  or  $k_{r-1} - k_r = 2$ . If  $k_{r-1} - k_r = 1$ ,  $B_i^r - T_i^r \leq 2$ . Otherwise we have  $|X_r| = k_r P_r + q_r$  and  $|X_{r-1}| = k_{r-1} P_{r-1} + q_{r-1}$ . We can show that  $q_r - q_{r-1} > 0$  if  $R < \sigma$ .

On each ring, EVENPGA first make steps of  $k + 1$  for  $q/8$  pins and then switch to steps of  $k$ . If  $q_r > q_{r-1}$ , we can divide the  $i$ -loop into three regions.

**Region I**  $j \leq q_{r-1}$ .  $B_i^r - T_i^r = k_r - k_{r-1} = 2$ .

**Region II**  $q_{r-1} < j \leq q_r$ .  $B_i^r - T_i^r = k_r - (k_{r-1} - 1) = 1$ .

**Region III**  $j > q_r$ .  $B_i^r - T_i^r = (k_r - 1) - (k_{r+1} - 1) = 2$ .

The argument is similar for  $k_{r-1} - k_r = 2$ . Hence in any case,  $1 \leq B_i^r - T_i^r \leq 2$ .  $\square$

From Lemma 5, we can bound the difference of neighboring side cuts. Let the flow through the left and right side cut of the grid cell  $g_i^r$  be  $L_i^r$  and  $R_i^r$  respectively. If the number of pins connected to a wire in the cell is  $a$ , we have the following equation.

$$L_i^r + B_i^r = T_i^r + R_i^r + a \Rightarrow R_i^r - L_i^r + a = B_i^r - T_i^r \quad (1)$$

Fig. 5 illustrates three types of cells based on the possible flows within the cell. We only need to investigate the change of cell type along the top center edge towards the top right corner because the package is symmetrical.

We start with the first cell in ring  $r$ . Cell  $g_1^r$  can be any type. Note that  $L_1^r = 0$ . Since  $B_1^r - T_1^r$  is at most 2,  $R_1^r = 0$ .  $a = 1$  if  $B_1^r - T_1^r = 1$  and  $a = 2$  otherwise.

Now consider the cell  $g_i^r$  and  $g_{i+1}^r$ . There are four cases.

**Case I**  $g_i^r$  is Type 3 and  $B_{i+1}^r - T_{i+1}^r = 1$ .  $R_{i+1}^r - L_{i+1}^r = 0$  because  $a = 1$  for a Type 3 cell. This means that  $g_{i+1}^r$  is also a Type 3 cell.

**Case II**  $g_i^r$  is Type 3 and  $B_{i+1}^r - T_{i+1}^r = 2$ . Since the left neighbor of  $g_{i+1}^r$  is Type 3 and since  $L_1^r = 0$  and  $L_i^r$  does not change between neighboring Type 3 cells (Case I),  $L_{i+1}^r = 0$ . Since  $g_i^r$  is Type 3,  $\pi_{i+1}^r$  must be connected within  $g_{i+1}^r$ . If  $R_{i+1}^r > 0$ , then  $\pi_{i+2}^r$  will not be connected because  $B_{i+1}^r - T_{i+1}^r - \text{Connection of } \pi_{i+1}^r = 1$ . It is impossible to connect this pin in the next cell,  $g_{i+2}^r$ , because the wire leaving the right side cut will block any possible connection in  $g_{i+2}^r$ . Therefore  $R_{i+1}^r$  must be 0.  $g_{i+1}^r$  is a Type 2 cell.

**Case III**  $g_i^r$  is Type 2.  $L_{i+1}^r = 0$  by Case II. Note that  $\pi_{i+1}^r$  is connected within  $g_i^r$ . Therefore  $g_{i+1}^r$  can only be a Type 1 cell.  $R_{i+1}^r - L_{i+1}^r = 1$  if  $B_{i+1}^r - T_{i+1}^r = 2$  and  $R_{i+1}^r - L_{i+1}^r = 0$  otherwise.

**Case IV**  $g_i^r$  is Type 1.  $g_{i+1}^r$  must be a Type 1 cell because  $\pi_{i+1}^r$  is already connected in  $g_i^r$ .  $R_{i+1}^r - L_{i+1}^r = 1$  if  $B_{i+1}^r - T_{i+1}^r = 2$  and  $R_{i+1}^r - L_{i+1}^r = 0$  otherwise.

We summarize the cases into the following lemma.

**Lemma 6** *The right neighbor of a cell can only be of certain type.*

1. The right neighbor of a Type 1 cell must be a Type 1 cell.
2. The right neighbor of a Type 3 cell can be a Type 3 cell or a Type 2 cell.
3. The right neighbor of a Type 2 cell is a Type 1 cell.

Fig. 4 shows the types of cells in the second ring. The chain breaks at the corner cell  $g_{13}^3$ . In general, if the first cell in the ring is Type 1, then all the cells up to top right corner is Type 1. If the first cell is Type 2, all the cells except the first is Type 1. If the first cell is Type 3, somewhere along the path the chain of Type 3 cells will end with a Type 2 cell (where  $B_i^r - T_i^r = 2$ ) and then after the Type 2 cell everything is Type 1.

From all four cases the maximum difference between  $R_i^r$  and  $L_i^r$  is 1. Therefore we have the following lemma.

**Lemma 7** *The change of flow between two neighboring side cuts is at most 1.*

From the four cases we can see that only Type 1 cells can have  $R_i^r - L_i^r > 0$ . So the maximum flow on side cuts from the top center to the top right corner is less than or equal to the number of Type 1 cells with  $B_i^r - T_i^r = 2$ . From the proof of Lemma 5, we know that  $B_i^r - T_i^r = 2$  happens only in Region I and III if  $q_r > q_{r-1}$  and in Region II if  $q_{r-1} > q_r$ .

If  $q_r > q_{r-1}$ , the number of cells where  $B_i^r - T_i^r = 2$  is equal to  $q_{r-1} + (k_{r-1} - q_r) < k_{r-1}$ . If  $q_{r-1} > q_r$ , the number of cells is equal to  $q_{r-1} - q_r < k_{r-1}$ . Therefore we have the following conclusion.

**Lemma 8** *The maximum flow of a side cut between rings  $r$  and  $r + 1$  is less than  $k_r$ .*

Now we have rather tight bounds on the cuts in the rings and on all the side cuts. To show that EVENPGA generates a even wiring distribution, we measure the densest cuts within the grid cells along a ring. Since the cuts within a ring has a uniform density (Lemma 3), the critical cut within a grid cell and its density is determined by the amount of side flow. There are only two competing cuts within the cell that can be the critical cut of the cell—the bottom cut and the diagonal cut which have the larger flow. At the center of an edge, the side flow is 0. The critical cut is  $(\pi_1^r, \pi_2^r)$ . This cut is critical because at least  $k_r - 1$  and at most  $k_r$  wires intersect it. At a corner cell, wires enter the cell from both the bottom and a side and leaves from the top and the other side. The diagonal cut, either  $(\pi_i^r, \text{prev}(\pi_{i+1}^r))$  or  $(\pi_{i+1}^r, \text{prev}(\pi_i^r))$ , become more critical because up to  $2(k_r - 1)$  wires may intersect it. The densities of the critical cuts of cells from the top center to the top right corner is bounded by the density of the critical cut of the cell at the center and that at the corner because the amount of side flow increase monotonically from center to corner. Therefore the maximum difference of densities of critical cuts across the ring is the difference of densities of critical cuts between a center cell and a corner cell. The following lemma summarizes the arguments.

**Lemma 9** *The critical cuts of ring  $r$  is either the bottom cut  $(\pi_1^r, \pi_2^r)$  or the diagonals  $(\pi_{P_r/8}^{r+1}, \text{prev}(\pi_{P_r/8+1}^{r+1}))$  and  $(\pi_{P_r/8+1}^{r+1}, \text{prev}(\pi_{P_r/8}^{r+1}))$ .*

The optimal wire distribution is such that the maximum difference of densities of the critical cuts in all the cells among a ring is less than 1.

**Theorem 2 (Even Wiring)** *EVENPGA generates a topological routing such that*

$$\Delta = \max_{\forall i} (D(\text{crit}(g_i^r))) - \min_{\forall i} (D(\text{crit}(g_i^r))) < 1$$

if  $k_r < 3 + 2\sqrt{2}$ .

**Proof:** By Lemma 9,  $\Delta = |D(\text{bottom cut}) - D(\text{diagonal})|$ . The density of the bottom cut of the cell in the center of the top edge is  $k_r$ . The density of the diagonal cut at the top right corner cell is less than or equal to  $2(k_r - 1)$ . Hence  $\Delta = |2(k_r - 1)/\sqrt{2} - k_r|$ . This is less than 1 if  $1 < k_r < 3 + 2\sqrt{2}$ .  $\square$

Since  $k_r > k_{r+1}$ , Lemma 9 implies that the critical cuts of the whole package is on ring 1.

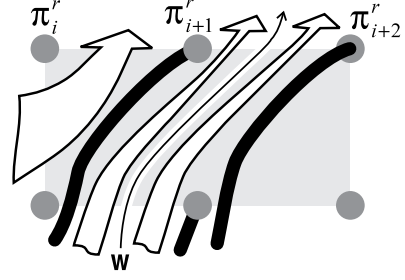


Fig. 6. A wire intersecting two cells between a pair of rings.

An optimally even distribution means the maximum density around a ring is minimal. Lemma 3 showed that the maximum difference of flow of an MTR created by EVENPGA is less than or equal to 1. Since  $k_1 = \lfloor T/8N \rfloor$ , the MTR of EVENPGA exactly equals the minimum and maximum flow requirements. Therefore we have following conclusion.

**Theorem 3** *If the MTR created by EVENPGA is routable, the maximum density of the critical cut is minimum if  $1 < k_1 < 3 + 2\sqrt{2}$ .*

## V. WIRE LENGTH ANALYSIS

Intuitively, the wire length generated by EVENPGA is short. MPA guarantees an MTR which means no detours for any net. In this section, we will derive a bound for the wire length of all nets.

First we find the bound on the number of side, bottom and top cuts of the grid cells a wire may intersect. Let  $\Gamma(w)$  be the total number of side, bottom and top cuts of cells  $w$  intersected. Since no detouring is allowed by the definition of MTR, a connection  $w = (\pi_i^r, p)$  must pass through exactly one cut on ring 1, 2,  $\dots$ ,  $r - 1$ . So  $\Gamma(w) \geq r - 1$  for all  $w$ .

Next we will show that a wire intersects at most one side cut between any pair of adjacent rings. To show that this is true, we need the following lemma:

**Lemma 10** *A grid cell  $g_i^r$  is always one of the three types as shown in Fig. 5.*

**Proof:** The proof can be derived easily by recognizing that the connecting wire always come from the left side cut instead from the bottom cut in Type 1 cells.  $\square$

By Lemma 10, the wire that makes the connection in a cell  $g_i^r$  always partitions the cell vertically into two disjoint parts. Hence any wire can only intersect at most one side cut between two bottom/top cuts. Therefore a wire may intersect two cells between a pair of adjacent rings by intersecting a side cut (Type I Intersection) or it may

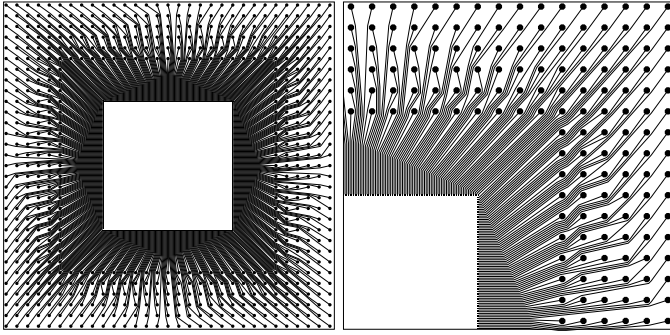


Fig. 7. 600 pin single-layer PGA and a quadrant.

intersect only one cell between a pair of adjacent rings by not intersecting any side cut (Type II Intersection).  $\Gamma(w) \leq 2(r-1)$  where  $r = \text{ringof}(w)$ . We define  $\Gamma_1(w)$  to be the number of Type I intersections and  $\Gamma_2(w)$  to be the number of Type II intersections. We have  $\Gamma_1(w) + 2\Gamma_2(w) = \Gamma(w)$  and  $\Gamma_1(w) + \Gamma_2(w) = r-1$  where  $r = \text{ringof}(w)$ . From this result we can state the following:

**Lemma 11** *The wire length of a wire  $w$  within the pin grid is less than or equal to  $\Gamma_1(w) + \sqrt{2}\Gamma_2(w)$ .*

**Proof:** Fig. 6 shows the wire in the cells. The maximum wire length of  $w$  is bounded by the diagonal length which is  $\sqrt{2}$  in Euclidean metric. Therefore if the wire  $w$  intersects  $\Gamma_1(w)$  cells orthogonally and  $\Gamma_2(w)$  cells diagonally, the wire length of  $w$  is bounded by  $\Gamma_1(w) + \sqrt{2}\Gamma_2(w)/2$ .  $\square$

Since the total number of cells a wire intersect does not exceed the number of rings beneath the pin of the wire,  $0 < \Gamma_1(w) < r-1$ . From Lemma 11 the bounds of a wire is  $r-1 < \text{length}(w) < \sqrt{2}(r-1)$ .

The taxicab wiring metric[1] is defined as  $(|y+x| + |y-x|)/2$  for a point  $(x, y)$ . The length of the diagonal of a square is the same as its side. The length of a wire intersecting a cell is 1 under this metric. Hence *all* wires connected to a given ring has length  $r-1$ . This is minimum because the minimum number of cells a wire intersects is also  $r-1$ . Hence we have the following theorem.

#### Theorem 4 (Minimum Wire Length)

*EVENPGA produces a topological routing where each wire is of minimum length in taxicab wiring metric.*

## VI. IMPLEMENTATION AND RESULTS

Fig. 7 is a 600 pin PGA routed with EVENPGA in the Surf environment. EVENPGA was implemented as a router module of Surf[5]. The run-time of EVENPGA is negligible compared to the generation of topological routing (MAKEMTR) and enforcing design rules.

## VII. CONCLUSION

This paper introduced MTR for PGA routing and gave an algorithm to produce a uniformly distributed and shortest wire length MTR. We have shown that the key to good topological routing is a good pin assignment. The routing can be used as a base for improvement for performance constraints such as delay and crosstalk.

## VIII. ACKNOWLEDGMENT

The authors wish to thank David Staepelaere, Jeffrey Su and Tal Dayan for their work on Surf. We also like to thank Joel Darnauer for helpful discussions on even wiring distribution.

## REFERENCES

- [1] F. M. Maley, *Single-layer wire routing and compaction*. Cambridge, MA: MIT Press, 1990.
- [2] C. Ying and J. Gu, "Automated pin grid array package routing on multilayer ceramic substrates," *IEEE trans. VLSI Systems*, vol. 1, no. 4, pp. 571-575, 1993.
- [3] C.-C. Tsai and S.-J. Chen, "Planar routing on a pin grid array package," in *Proc. 3rd Int'l Conf. CAD and Comp. Graphics*, (Beijing, China), pp. 439-445, August 1993.
- [4] J. Darnauer and W. W.-M. Dai, "Fast pad redistribution from periphery-io to area-io," in *Proc. IEEE Multi-Chip Module Conf.*, (Santa Cruz, CA), pp. 38-43, March 1994.
- [5] D. Staepelaere, J. Jue, T. Dayan, and W. W.-M. Dai, "Surf: a rubber-band routing system for multichip modules," *IEEE Design and Test Magazine*, December 1993.
- [6] W. W.-M. Dai, T. Dayan, and D. Staepelaere, "Topological routing in surf: Generating a rubber-band sketch," in *Proc. 28th Design Automation Conf.*, (Anaheim, CA), pp. 39-44, IEEE Computer Society Press, 1991.
- [7] W. W.-M. Dai, R. Kong, and M. Sato, "Routability of a rubber-band sketch," in *Proc. 28th Design Automation Conf.*, (Anaheim, CA), pp. 45-48, IEEE Computer Society Press, 1991.
- [8] R. Kong, "Incremental routability test for planar topological routing," Master's thesis, University of California, Santa Cruz, 1992.
- [9] D. Staepelaere, "Geometric transformations for a rubber-band sketch," Master's thesis, University of California, Santa Cruz, 1992.