A digital audio signal processor for cellular phone application

Jeongsik Yang , Chanhong Park

Department of Electrical Engineering
Korea Advanced Institute of Science and Technology
373-1 Kusong-dong,Yusong-ku,Taejon 305-701,Korea
Tel:+82-42-869-5455
Fax:+82-42-869-8055
e-mail:paul@angella.kaist.ac.kr
e-mail:chpark@tinkerbell.kaist.ac.kr

Beomsup Kim

Department of Electrical Engineering
Korea Advanced Institute of Science and Technology
373-1 Kusong-dong,Yusong-ku,Taejon 305-701,Korea
Tel:+82-42-869-3455
Fax:+82-42-869-8055

e-mail:bkim@eekaist.kaist.ac.kr

Abstract— A salient digital audio signal processor for mobile communication receiver is described in this paper. With this IC, the complete audio signal processing system of an AMPS or a TACS cellular phone is easily implemented. The processor can be also applied to cellular radio, high performance cordless telephone, etc. In this paper, as an example of application, the implementation of AMPS audio signal processing system is presented. To save the power consumption, some special consideration of the low power architectures has been made. The DSP core uses 4 stage pipelining without a routine memory access stage to reduce the power consumption and execution speed. The parallel calculations of data in the DSP and separated filter blocks also contribute to reduce the clock frequency and to save power. It also provides the power-down mode that turns off the IC except the internal bus interface in the standby mode. It uses 3.3V power supply, 10MHz 4-phase clock. The data sampling rate is 10K-samples per second.

I. Introduction

In the frequency modulation(FM) systems including the analog cellular phone system, some preprocessings are required for the input audio signal to reduce the noise and interference due to the channel and the demodulator[1]. Among them preemphasis/deemphasis and compressing/expanding are most important. Preemphasis and deemphasis are used to reduce the magnitude of the interference generated by FM demodulator. The interference tends to increase as the signal frequency gets higher. Therefore preemphasis and deemphasis are required to keep the SNR(Signal to Noise Ratio) same amount in the upper and lower band voice signal. Compressing and expanding are also required to reduce the channel noise and therefore improve the SNR at the receiver[1].

Although there are several IC's that implement these processes in analog techniques[2], digital implementation is considered in this paper because there are several advantages of the digital implementation. One of the key advantages is that the digital implementation makes the IC fully programmable. By programming the IC and changing the values in the control register, several special processing algorithms besides compressing/expanding can be easily implemented in the DSP. The architecture of the digital approach is designed for reducing power consumption. The three most important architectural considerations for the low power design are pipelining, parallelism, and power down mode. First, in this IC, four pipelined stages are used. Because the signal processing in this IC does not need many memory accesses unlike the conventional RISC(Reduced Instruction Set Computer) type DSP's, if there is a routine memory access in the pipelined stages, it wastes execution time and power. To avoid it, the memory access is not a separate stage in the pipelined stages. Second, to reduce the clock rate and save the power of the DSP core, the filter block is implemented separately, achieving parallelism[3]. Although the DSP core can perform the digital filtering with the increased clock rate, it will also make the power consumption increased. Therefore, the filters are separated from the DSP core and process the data fully in parallel. Third, the power-down mode is supported. When the system is in the standby mode, all the blocks in the IC except the bus interface are turned off, and only small amount of power is consumed. When in the normal mode, the blocks are turned on and the IC performs the signal processing.

Section II describes the overall flow of signal processing in AMPS application. The individual architecture of each block of the chip is explained in Section III. In section IV, the simulation results and the layout of the chip are presented. Finally, the conclusion of this paper is summarized in Section V.

II. Overall audio signal processing flow

The signal processing performed by this chip is divided into two parts, TX path and RX path. The signal flow of each part for AMPS application is shown in Figure 1.

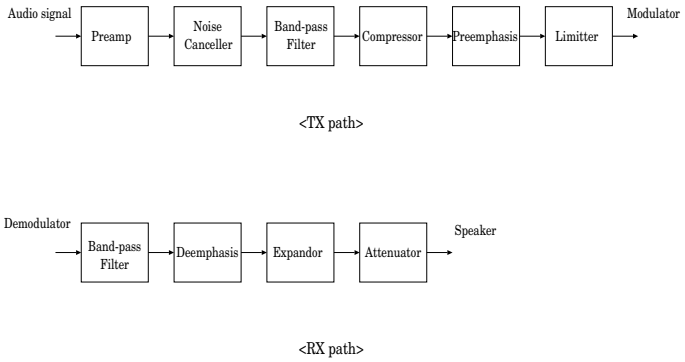

Figure 1: Signal flow in TX and RX path

Preemphasis and deemphasis are used to overcome the "colored" noise present in FM receivers, generated by FM demodulator. Since this noise gets worse at the upper voice band as shown in Figure 2, in order to keep the SNR in the lower and upper noise band equal, preemphasis and deemphasis are required. With the preemphasis filter, the voltage level of the upper voice band signal gets higher and the level of lower voice band gets lower. The deemphasis filter is actually an inverse filter of the preemphasis filter. As a consequence, the amplitude of the voice signal is not changed after preemphasis and deemphasis, but the noise amplitude generated by the demodulator in upper band decreases.

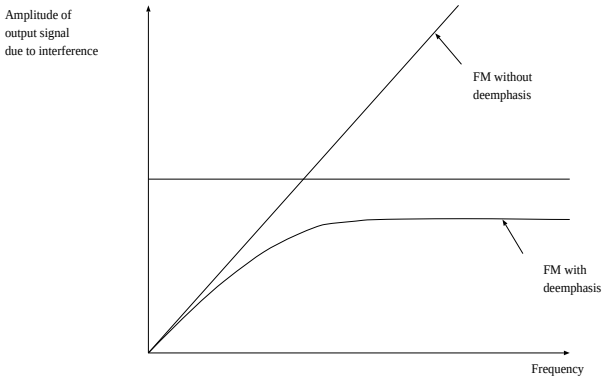

Figure 2: Amplitude of FM demodulator output due to the interference

The compressing/expanding are required to decrease the effect of the channel noise[1]. The expandor makes the low-level signal lower, and the high-level signal higher. The channel noise is usually low-level signal and the ratio of the noise component decreases after expanding. Because the voice signal should not be affected by the expanding, compressing is required in TX path.

In this IC, the preemphasis and deemphasis are realized by FIR filter and IIR filter respectively and the compressing and expanding are performed in the DSP block.

III. Architecture

Audio Signal Processor(ASP) is focused on the low power design for the cellular phone application. First, to achieve the low power IC, we exploit the parallelism and the pipelined architecture. The parallelism and the pipelining decrease the clock frequency of the chip, and as a result, the power dissipation decreases[3][4]. Second, to decrease the power dissipation further, we use the 3.3V supply voltage. As the supply voltage is lower, the power dissipation decreases[5]. Third, the power down mode is implemented to decrease the unnecessary power dissipation. When the chip is not used for a long time, it enters the power down mode where the power of the chip is turned off except the I^2C bus interface block. Finally, to reduce the unnecessary routine memory access, four stage pipelining is used unlike other DSP's. Figure 3 shows the ASP's block diagram.

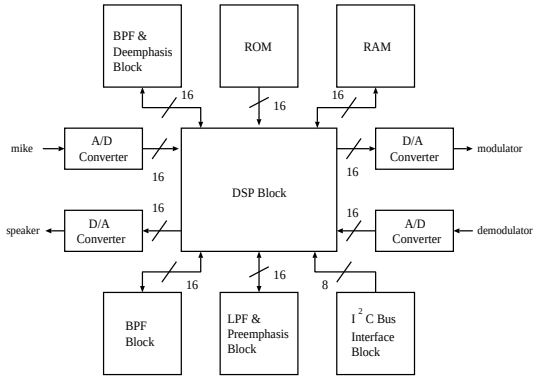

Figure 3: Chip block diagram

The ASP chip is divided into five functional blocks: the DSP core block, the filter block, the I^2C bus interface block, the I/O interface block, and the memory block. To achieve the parallelism, the chip uses the dedicated filter hardware in addition to the DSP core. The DSP core block executes the companding algorithm and controls the other blocks of the chip. The filter block performs the preemphasis algorithm, the deemphasis algorithm, and the band-pass filtering algorithm. Although the DSP core block can execute the algorithm of the filter block besides the companding algorithm, if it does, the clock frequency of the chip must increase and as a result, the power dissipation of the chip increases accordingly. I^2C bus interface block performs the communication with the other chip(data processor, control processor, etc)[2]. The memory block contains the signal processing program and the parameters of the algorithm. The I/O block performs the communication with the external elements. In the ASP chip, the memory mapped I/O method is used for the simplified addressing mode[6].

In this section, the architecture of the DSP core block is shown. Then, the filter block and the I^2C bus interface block are examined.

A. DSP core block

The DSP core is a 16-bit processor that uses a simplified instruction set and four stage pipelining. The DSP core uses the Harvard architecture for the efficient instruction fetch in the pipelined architecture[7]. It consists of a register file containing 16 general purpose registers, a 16-bit ALU, a 16-bit shifter, and a 32-bit multiplier. The division algorithm is implemented by software. The flag register stores the status of the previous instruction. To simplify the architecture, the memory operations are limited to load and store. Figure 4 shows the diagram of the DSP core block.

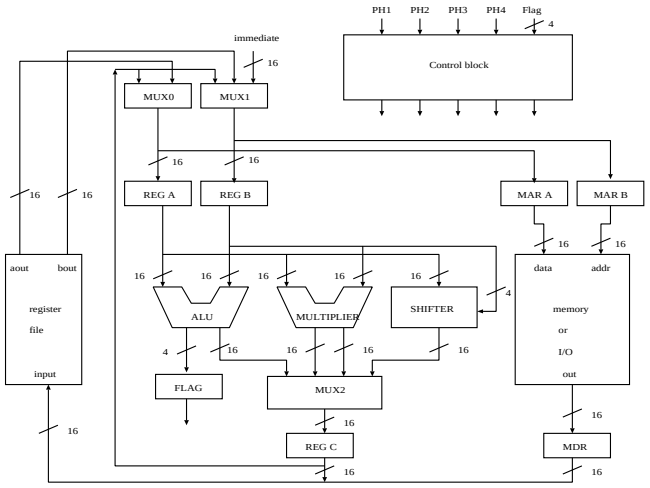

Figure 4: DSP core block

- Instruction format and set

The instruction set is designed to be very simple to decode so that only simple hardware is required for its execution. There are 30 instructions in the instruction set. Figure 5 shows the instruction format of the core processor.

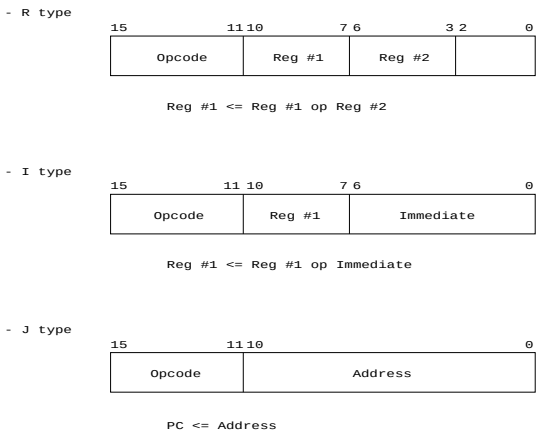

Figure 5: Instruction format

There are three types in the instruction format: R-type(Register type), I-type(Immediate type), and J-type(Jump type). R-type is made to perform the operation between two registers: ten ALU instructions, one data move instruction, one load instruction, one store instruction and one nop instruction. The results of the operations between the register1 and the register2 are stored to the register1 in the R-type instructions. The value of the register1 is used for the data and the value of the register2 is used for the address in the memory operations. I-type instructions operate between a register and an immediate data. Five ALU instructions, two interrupt instructions, one reset instruction and one data transfer instruction are I-type instructions. The operations between the register1 and the immediate data occur in I-type instructions and the results are stored to the register1. Six branch instructions and one jump instruction are J-type instructions. They consist of an opcode and an 11 bit target address for the branch operations. If the branch is taken, the program counter is changed to the 11 bit target address. There are some important benefits from using the simplied instruction set. First, simple circuits can be used to implement the instructions in hardware. As a consequence of it, the power dissipation of the chip decreases. Second, it needs small area to implement the function and the surplus area can be used to implement the other features.

- Pipelining

The DSP core uses a pipelined architecture for the low power strategy[3]. Each instruction is executed with 4 pipelined stages: IF(Instruction fetch), RF(Instruction decode and register fetch), EXE(Execution), and WB(Write back). Several DSP processors use 5 stage pipelining for the memory access: IF, RF, EXE, MEM, WB[8]. In this architecture, all the instructions except the memory related instructions waste the MEM stage. There are several benefits of using the four stage pipelining in this application. While the memory operations take about 30 percentages of the the total operations in the general DSP processors[8], only 8 percentages of the total program codes are the memory instructions in this application. Therefore, the 5 stage pipelining structure would waste the area and the power of the chip for this application. The 4 stage pipelining saves area and power and fits to our low power strategy. The controller is very simple for 4 stage pipelining and it allows to insert easily new functional block.

RegA, RegB, and RegC store the results of the previous stages. The instruction cache doesn't exist in the DSP core block because of its low speed memory access.

- Clocking

Unlike some other processors[9] that use a two-phase non-overlapping clock scheme, The DSP core block uses a

PH1	regfile selection signal ALU, shifter selection signal regC or mdr enable signal mux selection signal memory RD/WR signal
PH2	PC load signal IR2 load signal regfile load signal memory clk signal
PH3	IR1 load signal regC, mdr load signal psw load signal promgram rom clk signal
PH4	IR0 load signal regA, regB load signal marA, marB load signal

Figure 6: DSP core instruction flow

four-phase clock scheme for the efficient memory access. Figure 6 shows the control flows according to each clock.

- Interrupts

There are five interrupts in the DSP core block: Reset, DTMF, timer1, timer2, and timer3 interrupt. Reset interrupt is unmaskable. When reset interrupt occurs, all components are initialized. DTMF interrupt is maskable and it is used to generate DTMF signal for dialing. Timer1 and timer2 are all maskable. The compressing mode is switched to the expanding mode when timer1 interrupt occurs. The adverse action occurs at the timer2 interrupt. Timer3 interrupt is used to synchronize the DTMF signal. Interrupt vector table is from 0000H to 0004H and the interrupts perform long jump service[6].

B. Filter architecture

For the signal processing, three digital filters are required. They are TX band-pass filter, preemphasis filter, and deemphasis filter. The band-pass filter and the preemphasis filter are implemented using a FIR filter architecture and the deemphasis filter is an IIR filter[10][11]. Because the number of the tabs of all filters are fairly large, a salient architecture is necessary. Instead of using many multiplier, ROM, RAM and some address control logic are used. The architecture of the FIR filter is shown in Figure 7. The ROM and RAM are used to store the coefficients and the temporal values produced by adder and multiplier, respectively. As a result, only one multiplier and one adder are used in each filter. Though it requires clock cycles as many as the number of tabs for an output produced, about 1000 clock cycles are available for one sampled signal, hence this architecture is adequate for this application.

C. I^2C bus interface block

The important purpose of the I^2C bus interface block is the communication with the other chip(data processor, control processor, etc)[2]. All control informations are transferred through the I^2C bus of the system. There are two lines in the I^2C bus. One is the clock line(SCL), and the other is the data line(SDL). The data is synchronized with the clock of the SCL. The data format is composed of a start bit, 8 bit address, an acknowledge bit, 8 bit data, an acknowledge bit, and an stop bit. There are three types in the access mode: quick access mode, address access mode, and test mode. In the quick access mode the low 5 bits of the first data byte is directly inserted into the register of the I^2C bus interface block. The low 4 bits of the first data bytes are the address of the register in the address access mode and the next data byte is transferred into the indicated register. The test mode is used only for the test.

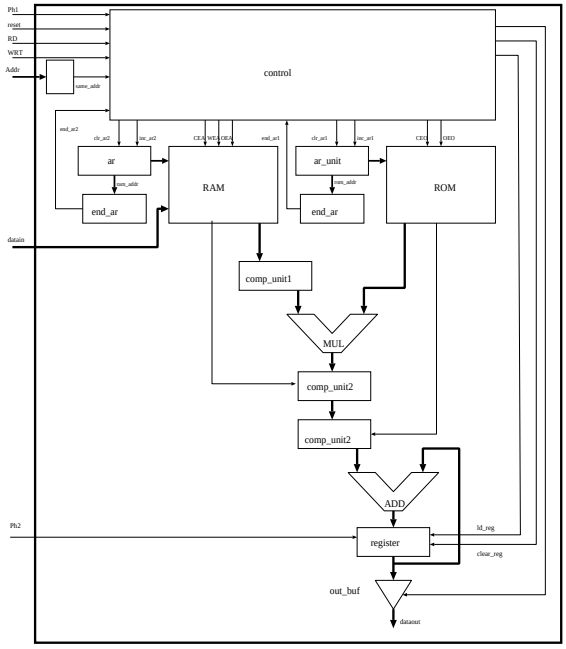

Figure 7: Schematic of FIR filter

IV. Simulation

The ASP is designed with the verilog HDL(Hardware Description Language). The design follows the top-down design method. First, the specification and the architecture of the ASP chip are decided. Next, it is decided whether each block should be implemented with hardware or software. Then, the interface of each block is decided, the verilog coding is performed correspondingly and the code is simulated by a verilog simulator. The verified block is implemented in 0.8μm CMOS. Post-layout simulation has been finished and the functions and performance are verified. The ASP chip uses a 10MHz clock and is composed of the 25,000 gates. It has 94 pins and its area is 6.3x6.3mm^2 including pads. The estimated power dissipation of the DSP core block is 75mW on 3.3V Vdd

and the power dissipation of the filter block is 120mW on 3.3V Vdd. In the power down mode, the total power dissipation of the chip is 1mW on 3.3V Vdd. Figure 8 shows the layout of the chip.

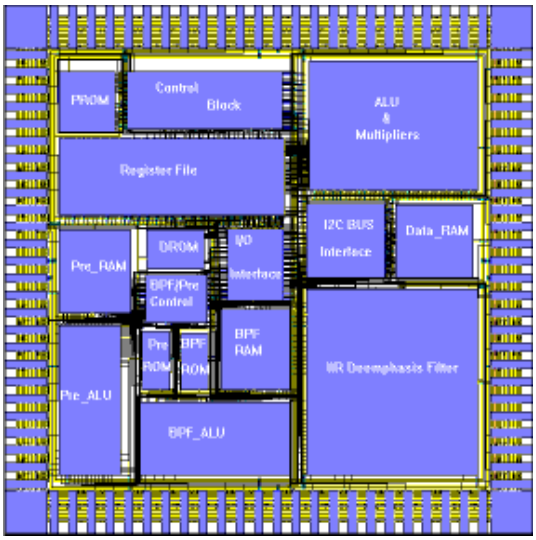

Figure 8: the ASP's layout

V. Conclusion

The Audio Signal Processor has been described in the previous chapters. The ASP uses the parallelism and the 4 stage pipelining and power down mode for the low power applications. From the estimated power dissipation, we can conclude that the parallelism, the 4 stage pipelining, reducing unnecessary memory access and the low supply voltage save the power of the chip. Also, the power down mode of the chip prevents the chip from dissipating unnecessary power when the chip is not used for a long time. The low power dissipation of the chip is adequate for the portable applications.

VI. Acknowledgements

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