[Panel Discussion]

Design Automation 2000—Challenges for the Gigabit Era

Moderator: Richard K. Wallace, EE Times, A CMP Publication, USA
Organizer: Kenji Yoshida, Toshiba Corp., Japan

Between now and the end of this decade the complexity of electronic systems will rise at an unprecedented rate, with silicon feature sizes shrinking toward 0.10 micron and circuit densities crossing the one-gigabit threshold for the first time. This leap in silicon and system complexity will usher in a new generation of high performance computer, communication, consumer and industrial electronic products.

But the Gigabit Era also poses a huge challenge to electronic design automation (EDA) tool users, developers and vendors. Keeping pace with new design technology is just part of the challenge. Increasingly in tomorrow’s Gigabit Era, matching and adapting new design methodologies to the fast pace of silicon and system evolution will prove equally challenging.

Key technology drivers in the Gigabit Era will be developments of higher and higher levels of design abstraction, more design reuse, faster design verification, and the linking of logical and physical design.

Market drivers will be increased pressure to bring enormously complex products to market sooner and faster. Expectations that these designs contain zero errors will intensify.

Guided by presentations from six of the industry’s top EDA participants, the “Design Automation 2000—Challenges for the Gigabit Era” panel will explore the impact of rising technology and market complexity on the design automation community of tool users, developers and EDA vendors. The leading vendors will share their vision of the trends and directions driving the base technologies in chip, board and system level EDA. The panelists will also plot their own roadmaps showing how changes in design methodology, business infrastructure and new development paths will pave the way into tomorrow’s Gigabit landscape.

Panel Members:

Joseph B. Costello - Cadence Design Systems, Inc., USA
Jeffrey H. Edson - Intergraph Electronics, USA
Aart J. de Geus - Synopsys, Inc., USA
Alan J. Hanover - Viewlogic Systems, Inc., USA
Jinya Katsube - ZUKEN, Inc., Japan
Walden C. Rhines - Mentor Graphics Corp., USA