7th International Symposium on High-Level Synthesis

Niagara-on-the-Lake, Ontario, Canada
May 18-20, 1994
Proceedings of the

Seventh International Symposium on High-Level Synthesis

May 18–20, 1994
Niagara-on-the-Lake, Ontario, Canada

Sponsored by

The IEEE Computer Society Technical Committee on Design Automation
The Association for Computing Machinery Special Interest Group on Design Automation (SIGDA)

In cooperation with

IFIP Workgroups 10.2 and 10.5

With corporate support by

Canadian Microelectronics Corporation
Waterloo Institute for Computer Research
Bell-Northern Research

IEEE Computer Society Press
Los Alamitos, California
Washington • Brussels • Tokyo
Table of Contents

Message from the Program Chair................................................................. vii
Steering Committee................................................................................. viii
Technical Committee................................................................................ ix

Invited Talk: Hardware/Software Co-Verification in ATM........................... 1
Giovanni Mancini, Bell-Northern Research, Ottawa, Canada

Session 1: Hardware/Software Systems

Session Chair: Robert Hum, Cadence Design Systems, Inc.

A Methodology for Simulation and Synthesis of Mixed Hardware/Software Systems (talk only)................................................................. 10
A. Kalavade and E.A. Lee

Instruction Set Definition and Instruction Selection for ASIPs..................... 11
J. Van Praet, G. Goossens, D. Lanneer, and H. De Man

Data Routing: A Paradigm for Efficient Data-Path Synthesis and Code Generation................................................................. 17
D. Lanneer, M. Cornero, G. Goossens, and H. De Man

Timing Analysis for Synthesis in Microprocessor Interface Design ............. 23
M.A. Escalante and N.J. Dimopoulos

Applications of Attributed-Behavior Synthesis......................................... 29
L.F. Arnstein and D. Thomas

Session 2: Estimation and Scheduling

Session Chair: Peter Duzy, Siemens AG

Computing Lower Bounds on Functional Units before Scheduling............... 36
S. Chaudhuri and R.A. Walker

Timing Estimation for Behavioral Descriptions........................................ 42
D. Mintz and C. Dangelo

Efficient Timing Constraint Derivation for Optimal Retiming High Speed Processing Units................................................................. 48
A. van der Werf, J.L. Van Meerbergen, E.H.L. Aarts,
W.F.J. Verhaegh, and P.E.R. Lippens

SMASH: A Program for Scheduling Memory-Intensive Application-Specific Hardware................................................................. 54
P. Gupta and A.C. Parker

Ensemble Representation and Techniques for Exact Control-Dependent Scheduling................................................................. 60
I. Radivojevic and F. Brewer

Panel Session: Is High-Level Synthesis Marketable?.................................. 66

Invited Talk: State-of-the-Art Compiler Optimization.................................. 67
Kenneth Zadeck, IBM Hawthorn Research Center, NY

Session 3: Retargetable Code Generation

Session Chair: Dominique Genin, European Development Center

An Integrated Approach to Retargetable Code Generation............................ 70
T. Wilson, G. Grewal, B. Halley, and D. Banerji
Bit-Alignment for Retargetable Code Generators ................................................. 76
  K. Schoofs, G. Goossens, and H. De Man

Code Generation for a DSP Processor .......................................................... 82
  W.-K. Cheng and Y.-L. Lin

Retargetable Assembly Code Generation by Bootstrapping ............................. 88
  R. Leupers, W. Schenk, and P. Marwedel

CodeSyn: A Retargetable Code Synthesis System (talk only) ......................... 94
  P.G. Paulin, C. Liem, T.C. May, and S. Sutarwala

Session 4: Verification, Test, and Fault-Tolerant Systems

  Session Chair: Mike McFarland, Boston College

Concurrent Testing in High-Level Synthesis ................................................. 96
  R. Singh and J. Knight

Testing Two-Phase Transition Signaling Based Self-Timed Circuits
  in a Synthesis Environment ........................................................................ 104
  P. Kadva and V. Akella

A Hybrid Numeric/Symbolic Program for Checking Functional and Timing
  Compatibility of Synthesized Designs .......................................................... 112
  C.-T. Chen and A.C. Parker

A Divide-and-Conquer Approach for Asynchronous Interface Synthesis ............ 118
  R. Puri and J. Gu

Rapid Prototyping of Fault-Tolerant VLSI Systems ......................................... 126
  R. Karri, K. Hogstedt, and A. Orailoglu

Panel Session: ASICs vs ASIPs ....................................................................... 132

Session 5: Control, Datapath, and Interface Synthesis

  Session Chair: Rich Cloutier, Cadence Design Systems, Inc.

Specification of Interface Components for Synchronous Data Paths .............. 134
  P. Gutberlet and W. Rosenstiel

Global Node Reduction of Linear Systems Using Ratio Analysis .................... 140
  M. Shelia and E.H.-M. Sha

A Specification Invariant Technique for Operation Cost Minimisation
  in Flow-Graphs ......................................................................................... 146
  M. Janssen, F. Catthoor, and H. De Man

Controller and Datapath Trade-Offs in Hierarchical RT-Level Synthesis ........ 152
  D.S. Rao and F.J. Kurdahi

How Datapath Allocation Affects Controller Delay ........................................ 158
  S.C.-Y. Huang and W.H. Wolf

An Algorithm for the Allocation of Functional Units from Realistic
  RT Component Libraries ............................................................................. 164
  R. Ang and N. Dutt

Author Index ................................................................................................. 171
Message from the Program Chair

This Symposium is the seventh in a series of high-quality technical forums. It is oriented towards design automation professionals and presents the latest results in emerging synthesis and system design technologies, including advances in behavioral synthesis algorithms, application-specific synthesis, high-level estimation, as well as advanced test and verification approaches.

This year marks two important new developments in the history of this meeting:
- The promotion of the meeting’s status from a Workshop to a full fledged Symposium.
- The appearance of the first official IEEE Proceedings. This further enhances the credibility of the Symposium and allows a broader dissemination of the innovative research and development it represents.

The 1994 program reflects the perceived importance of the following new and emerging technologies:
- Hardware/software co-design
- Retargetable compiler technology, with particular emphasis on application-specific embedded processors
- Application-specific behavioral synthesis
- Estimation and its role in architectural exploration

The continued evolution of the program in these strategic new directions is eloquent proof of the Symposium’s relevance to state-of-the-art synthesis and system design technologies.

We had a total of 67 paper submissions from Asia, Europe and North America. The program committee selected 26 papers from these submissions, following a rigorous review process. Each paper was evaluated independently by five reviewers. Reviewers were only assigned papers in their stated areas of expertise. A first round of independent reviews allowed us to partition the papers into “definite accepts,” “definite rejects,” and “potential accepts.” The latter were eligible for a second review round. This was done at a general meeting where nearly all of the twenty-five reviewers were present. For each paper, reviewers were given the opportunity to revise their ratings based on a consensus-building group discussion. The papers were then ranked a second time using their new marks, and the top papers were accepted. As always, many good papers did not make the program since we wanted to keep the program to a 2½-day schedule. Furthermore, we accepted somewhat fewer papers than in previous years, in order to guarantee that our first proceedings reflect truly high-quality, innovative work.

In conclusion, I would like to take this opportunity to thank the Organizing Committee, the Program Committee, the Session Chairs, and the Panelists for helping to make this Symposium a success. I would also like to thank all the authors for submitting high-quality work which, for the first time, will be broadly available to the general research and engineering community as a formal IEEE Proceedings.

Pierre G. Paulin
Program Chair
Steering Committee

Workshop Chairperson
Dan D. Gajski
Department of Computer Science
University of California, Irvine
Irvine, CA 92717
USA

Technical Program Chairperson
Pierre G. Paulin
BNR
P.O. Box 3511, Station “C”
Ottawa, Ontario K1Y 4H7
Canada

Organization Chairperson
Farhad Mavaddat
Department of Computer Science
University of Waterloo
Waterloo, Ontario N2L 3G1
Canada

Publicity Chairperson
Cathy Geboleys
Department of Electrical Engineering
University of Waterloo
Waterloo, Ontario, N2L 3G1
Canada

Panel Chairperson
Leon Stok
IBM
P.O. Box 218
Yorktown Heights, NY 10598
USA

Benchmark Coordinator
Nikil Dutt
Department of Computer Science
University of California, Irvine
Irvine, CA 92717
USA
Technical Program Committee

M. Balakrishnan  
*IIT Delhi*  
*India*

Lev Markov  
*Racal-Redac*  
*USA*

Raul Camposano  
*Synopsys*  
*USA*

Peter Marwedel  
*University of Dortmund*  
*Germany*

Giovanni De Micheli  
*Stanford University*  
*USA*

Yukihiro Nakamura  
*NTT*  
*Japan*

Guang Gao  
*McGill University*  
*Canada*

Alice C. Parker  
*University of Southern California*  
*USA*

Cathy Gebotys  
*University of Waterloo*  
*Canada*

Jan Rabaey  
*University of California, Berkeley*  
*USA*

Emil Girczyc  
*Synopsys*  
*USA*

Wolfgang Rosenstiel  
*University of Tuebingen*  
*Germany*

Gert Goossens  
*IMEC*  
*Belgium*

Gabrielle Saucier  
*INPG/CSI*  
*France*

Yu-Chin Hsu  
*University of California, Riverside*  
*USA*

John P. Shen  
*Carnegie Mellon University*  
*USA*

Ahmed Jerraya  
*INPG*  
*France*

Leon Stok  
*IBM*  
*USA*

Fadi Kurdahi  
*University of California, Irvine*  
*USA*

Donald Thomas  
*Carnegie Mellon University*  
*USA*

Ed Lee  
*University of California, Berkeley*  
*USA*

Kazutoshi Wakabayashi  
*NEC*  
*Japan*

Steve Y.-L. Lin  
*Tsing Hua University*  
*Taiwan*

Wayne Wolf  
*Princeton University*  
*USA*

Paul Lippens  
*Philips*  
*The Netherlands*
Author Index

<table>
<thead>
<tr>
<th>Name</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aarts, E.H.L.</td>
<td>48</td>
</tr>
<tr>
<td>Akella, V.</td>
<td>104</td>
</tr>
<tr>
<td>Ang, R.</td>
<td>164</td>
</tr>
<tr>
<td>Arnstein, L.F.</td>
<td>29</td>
</tr>
<tr>
<td>Banerji, D.</td>
<td>70</td>
</tr>
<tr>
<td>Brewer, F.</td>
<td>60</td>
</tr>
<tr>
<td>Catthoor, F.</td>
<td>146</td>
</tr>
<tr>
<td>Chaudhuri, S.</td>
<td>36</td>
</tr>
<tr>
<td>Chen, C.-T.</td>
<td>112</td>
</tr>
<tr>
<td>Cheng, W.-K.</td>
<td>82</td>
</tr>
<tr>
<td>Cornero, M.</td>
<td>17</td>
</tr>
<tr>
<td>Dangelo, C.</td>
<td>42</td>
</tr>
<tr>
<td>De Man, H.</td>
<td>11, 17, 76, 146</td>
</tr>
<tr>
<td>Dimopoulos, N.J.</td>
<td>23</td>
</tr>
<tr>
<td>Dutt, N.</td>
<td>164</td>
</tr>
<tr>
<td>Escalante, M.A.</td>
<td>23</td>
</tr>
<tr>
<td>Goossens, G.</td>
<td>11, 17, 76</td>
</tr>
<tr>
<td>Grewal, G.</td>
<td>70</td>
</tr>
<tr>
<td>Gu, J.</td>
<td>118</td>
</tr>
<tr>
<td>Gupta, P.</td>
<td>54</td>
</tr>
<tr>
<td>Gutberlet, P.</td>
<td>134</td>
</tr>
<tr>
<td>Halley, B.</td>
<td>70</td>
</tr>
<tr>
<td>Hogstedt, K.</td>
<td>126</td>
</tr>
<tr>
<td>Huang, S.C.-Y.</td>
<td>158</td>
</tr>
<tr>
<td>Janssen, M.</td>
<td>146</td>
</tr>
<tr>
<td>Kalavade, A.</td>
<td>10</td>
</tr>
<tr>
<td>Karri, R.</td>
<td>126</td>
</tr>
<tr>
<td>Knight, J.</td>
<td>96</td>
</tr>
<tr>
<td>Kudva, P.</td>
<td>104</td>
</tr>
<tr>
<td>Kurda, F.J.</td>
<td>152</td>
</tr>
<tr>
<td>Lanneer, D.</td>
<td>11, 17</td>
</tr>
<tr>
<td>Lee, E.A.</td>
<td>10</td>
</tr>
<tr>
<td>Leupers, R.</td>
<td>88</td>
</tr>
<tr>
<td>Lier, C.</td>
<td>94</td>
</tr>
<tr>
<td>Lin, Y.-L.</td>
<td>82</td>
</tr>
<tr>
<td>Lippens, P.E.R.</td>
<td>48</td>
</tr>
<tr>
<td>Mancini, G.</td>
<td>1</td>
</tr>
<tr>
<td>Marwedel, P.</td>
<td>88</td>
</tr>
<tr>
<td>May, T.C.</td>
<td>94</td>
</tr>
<tr>
<td>Mintz, D.</td>
<td>42</td>
</tr>
<tr>
<td>Oraloglu, A.</td>
<td>126</td>
</tr>
<tr>
<td>Parker, A.C.</td>
<td>54, 112</td>
</tr>
<tr>
<td>Paulin, P.G.</td>
<td>94</td>
</tr>
<tr>
<td>Puri, R.</td>
<td>118</td>
</tr>
<tr>
<td>Radiojovic, I.</td>
<td>60</td>
</tr>
<tr>
<td>Rao, D.S.</td>
<td>152</td>
</tr>
<tr>
<td>Rosenstiel, W.</td>
<td>134</td>
</tr>
<tr>
<td>Schenk, W.</td>
<td>88</td>
</tr>
<tr>
<td>Schoofs, K.</td>
<td>76</td>
</tr>
<tr>
<td>Sha, E.H.-M.</td>
<td>140</td>
</tr>
<tr>
<td>Sheliga, M.</td>
<td>140</td>
</tr>
<tr>
<td>Singh, R.</td>
<td>96</td>
</tr>
<tr>
<td>Sutarwala, S.</td>
<td>94</td>
</tr>
<tr>
<td>Thomas, D.</td>
<td>29</td>
</tr>
<tr>
<td>Van der Werf, A.</td>
<td>48</td>
</tr>
<tr>
<td>Van Meerbergen, J.L.</td>
<td>48</td>
</tr>
<tr>
<td>Van Praet, J.</td>
<td>11</td>
</tr>
<tr>
<td>Verhaegh, W.F.J.</td>
<td>48</td>
</tr>
<tr>
<td>Walker, R.A.</td>
<td>36</td>
</tr>
<tr>
<td>Wilson, T.</td>
<td>70</td>
</tr>
<tr>
<td>Wolf, W.H.</td>
<td>158</td>
</tr>
</tbody>
</table>