Built-in Self-Test and Fault Diagnosis of Fully Differential Analogue Circuits*

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Abstract

An approach to the test and diagnosis of fully differential analogue circuits is described in this paper. The test approach is based on off-line monitoring via an analogue BIST observer the inputs of the operational amplifiers in the circuit. The analogue BIST can detect both hard and soft faults. Diagnosis resolution is improved by also monitoring the outputs of the operational amplifiers. Faulty components can then be located and the actual defective value of a faulty passive component determined.

1 Introduction

In the last few years, analogue and mixed-signal integrated circuits have grown in importance, representing nowadays a relevant part of the market both in terms of production volume and of applications [1]. The integration of this type of circuits impacts not only design, but testing and diagnosis as well. As a consequence, various design for testability (DFT) and built-in self-test (BIST) schemes have been proposed.

To our knowledge, BIST approaches are limited to an analogue scan path that provides observability of circuit internal points (Analogue-BIST [2]), to the use of pattern generators and signature analysers associated, respectively, with a digital-to-analogue and an analogue-to-digital converter for testing the analogue parts of mixed-signal circuits (Hybrid-BIST [3]), and to a technique for verifying via special detectors whether or not the tested parameters (gain, phase, etc.) are within an acceptance window (Translation-BIST [4]).

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Given that the previous BIST techniques either are not adequate, or will fail to exploit the inherent redundancy of fully differential circuits, in this paper we propose a suitable analogue BIST structure for off-line testing and diagnosis of this class of circuits.

2 Testing Fully Differential Circuits

The widespread use of fully differential circuits is mainly justified by the fact that they achieve high performance requirements, such as high linearity and high signal-to-noise ratio. In addition, the application range of this class of circuits [5] covers continuous filtering (transconductor filters), switched-capacitor filters, algorithmic analogue-to-digital converters, etc.

The test of fully differential circuits has initially been addressed in [6], where the problems faced while designing self-checking mixed-signal integrated circuits were identified. More recently, the design of checkers for concurrent error detection in fully differential and duplicated circuits has been presented [7].

While on-line monitoring is usually necessary for high safety systems, the hardware overhead, the signal degradation and the loss in diagnosis resolution may be important. Therefore, for circuits which do not require such an on-line testing capability, an off-line test approach should overcome these drawbacks.

3 Off-line Test Strategy

Fully differential analogue circuits are built from individual stages connected by differential signals. A differential signal S represents two physical signals Sp and Sn which are carried by different wires and which verify in the AC domain $Sp + Sn = 0$. Thus, the small signals Sp and Sn appear with both positive and negative polarities with respect to analogue ground. The test strategy is based on observing the balance (Sp + Sn) of these signals. The 3-stage biquadratic filter of figure 1 is used to illustrate the test strategy.

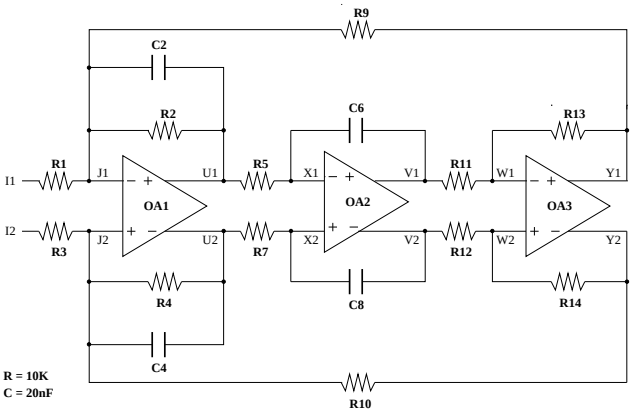

Figure 1: Fully Differential Biquadratic Filter

Each stage consists of an active fully differential amplifier and some passive components. The outputs of a non-saturated fully differential amplifier with high gain **G** verify

$$\left.\begin{array}{rcl} \mathrm{Out}^+ & = & G\,(\mathrm{In}^+ - \mathrm{In}^-) \\ \mathrm{Out}^- & = & -\mathrm{Out}^+ \end{array}\right\} \qquad (1)$$

and in a fully differential circuit the amplifier inputs are at a virtual ground ($\mathrm{In}^+ \approx 0$ and $\mathrm{In}^- \approx 0$). In figure 1, the input I to the circuit corresponds to a differential signal I (represented by I1 and I2), the inputs of all the operational amplifiers are at a virtual ground during correct operation and the outputs of the amplifiers must represent differential signals.

The two main classes of faults commonly used for analogue circuits – catastrophic (or hard) and parametric (or soft) faults – are considered. We assume a complete set of single hard faults in the operational amplifiers. These faults include three types of MOS transistor shorts (gate-source, gate-drain and source-drain) and three types of opens (gate, source and drain). For the passive components, capacitor and resistor shorts and opens are taken into account. Soft faults in passive components are also considered. Finally, differential faults (such as shorts between differential nodes) cannot be detected and they must be prevented by considering appropriate layout rules.

A deviation of a passive component from its nominal value can only be observed by balance checking in the inputs of the amplifier to which the component is connected to. For example, a fault in R2 in figure 1 will result in a value for J1 and J2 different from analogue ground. Since the amplifier is not faulty, J1 $\approx$ J2. The outputs of all amplifiers will still be differential (ΔU2 $\approx -\Delta$U1) and the fault in R2 will only be observable by balance checking in node J.

Figure 2 represents the effect of hard faults in passive components connected to node J. The common mode signal J1+J2 is made relative to the input differential signal I1-I2. These curves are valid if the amplifiers do not reach saturation for the input voltage applied. For each fault, there is a frequency region in which the common mode signal can be observed.

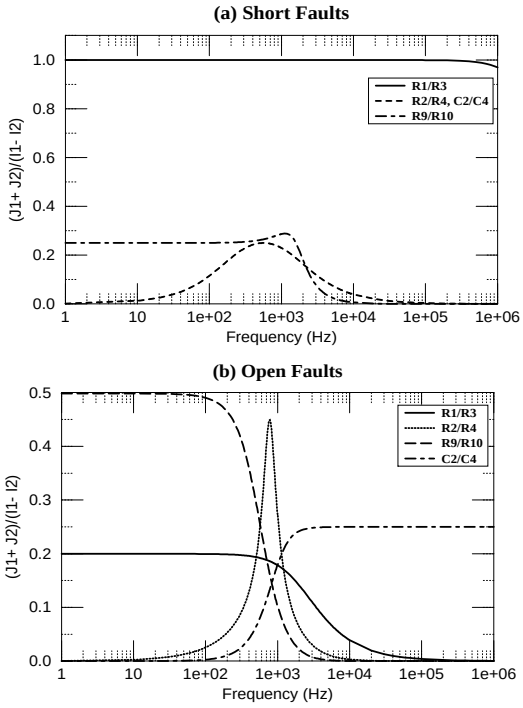

Figure 2: Effect of Hard Faults on node J

In the case of a faulty amplifier, two classes of faults must be considered. The first class includes faults which involve the gates of the transistors in the input differential pair of the amplifier. These faults include two shorts (gate-drain and gate-source) for each input transistor. We have found that these faults always result in a non-differential signal at the input of the amplifier. The amplifier is saturated and the outputs are stuck at Vdd and DC ground, respectively. This fault is propagated to the rest of the circuit and results in the saturation of the other amplifiers. The outputs of the circuit are then stuck at Vdd and DC ground.

The second class of amplifier faults include hard faults in all components except the faults in the previous class. We have found by fault simulation that all faults which affect the behaviour of the amplifier result in an asymmetry in the differential outputs. Some 8% of faults do not change at all the operational amplifier behaviour. These faults have been examined in a multiple fault context and the output behaviour produced

by any double fault was found to fall into one of the two previous classes of faults. Finally, it can readily be shown for the circuit of figure 1 that if the output of an operational amplifier is not differential, its input cannot be differential either.

4 Analogue BIST

The analogue BIST structure proposed is shown in figure 3. Differential nodes in the signal path are observed via an analogue multiplexer.

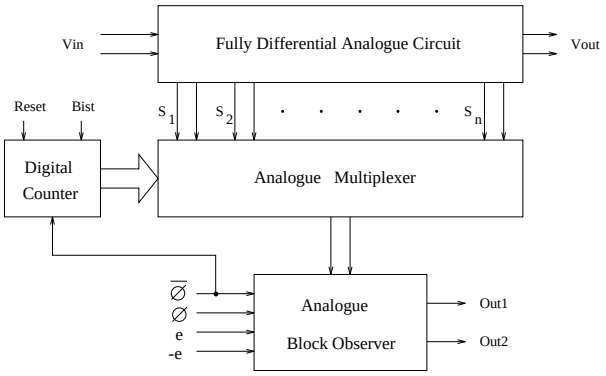

Figure 3: BIST for Fully Differential Circuits

Signals *Bist-Reset* control the BIST circuitry. For 0-0 the BIST is disabled. When *Reset* is set to 1, the counter is cleared and the multiplexer selects the differential signal S1 which corresponds to Vin. Thus, for 1-1 a test for the analogue observer can be carried out since Vin is seen at its inputs. For 0-1, which clears the counter, followed by 1-0, the test of the fully differential circuit is carried out. It must be noted that the counter and the analogue multiplexer are sufficiently exercised during testing.

The analogue block observer is shown in figure 4. It operates as a sample-and-compare circuit as follows:

- during phase ϕ, the operational amplifiers actuate as voltage followers. The differential signals Sp and Sn selected by the multiplexer are stored in the capacitors of the decoding circuit.

- during phase $\overline{\phi}$, the operational amplifiers actuate as comparators. The decoder adds Sp and Sn and the result is compared with the acceptance window -e and e. For a code signal, the output *out1-out2* gives 10 and non-code signals give either 00 or 11. In addition, a new differential node is selected during $\overline{\phi}$ by incrementing the digital counter.

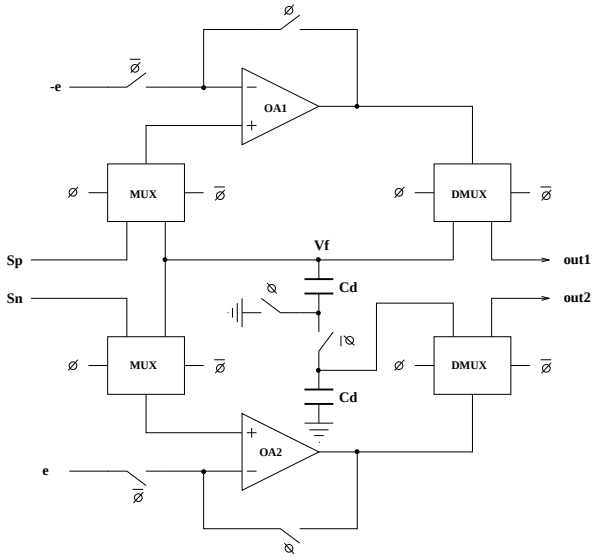

Figure 4: Sample-and-Compare Block Observer

The capacitances at the inputs of the amplifiers have an appreciable effect on the final value of the decoding circuit. The final value Vf of the addition after an initial transient in the decoding circuit can be calculated as

$$V_f = \frac{1 + 2\,\frac{Cg}{Cd}}{1 + 4\,\frac{Cg}{Cd}}\,(Sp + Sn)$$

where Cg models the input capacitance of the amplifiers. For Cd=10 Cg, this gives $V_f = 0.86(Sp + Sn)$. This factor must also be applied to the values of the tolerance window $[-e, e]$ in order to increase the precision of the circuit. Circuit precision is limited by the effects of charge injection in the switches and operational amplifier offsets.

The performance of the analogue observer is shown in figure 5 (with Cd=10pF). The analogue ground is set to 2.5 DC volts. *Sn* is kept at an AC value of -1 volt (1.5 DC). A step function from 1.06 volts to 1.14 volts is applied to *Sp* after 4 μ-seconds with an increase of 10 milivolts each 2 μ-seconds. The tolerance window is set to $[-86, 86]$ milivolts. A testing frequency of 0.5 MHz is used in order to show the effect of the slew rate of the amplifiers. The output signals *out1-out2* are EXNORed to produce an error signal which is stored in a master-slave flip-flop (thus, a change in the error signal generated during phase $\overline{\phi}$ is shown at the beginning of phase ϕ with an additional delay of 1 μ-second).

For a code signal, the outputs of the amplifiers OA1 and OA2 must be at Vdd and ground, respectively,

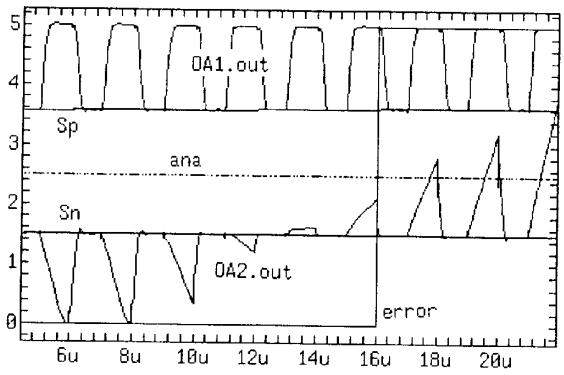

Figure 5: Analogue Observer Simulation

during the comparison. The output of amplifier OA2 moves towards Vdd during the comparison after 1.1 volts in Sp, as required. It must be observed that the speed of change is initially too slow (for the frequency of 0.5 MHz) to reach the threshold value of the EXNOR gate and thus signaling an error.

5 Fault Diagnosis

A procedure for the diagnosis of a single fault in a differential circuit is presented next. For passive components, the location of hard faults is seen as a particular case of the location of soft faults. As discussed in section 3, a fault in a circuit component will only affect the balance of some of the differential signals in the circuit. For the circuit of figure 1, table 1 classifies the components according to the signals affected.

Case	Faulty Component	Affected Signal
I	R1, R3, C2, R2, R4, C4, R9, R10	J
II	R5, R7, C6, C8	X
III	R11, R12, R13, R14	W
IV	OA1	J, U
V	OA2	X, V
VI	OA3	W, Y

Table 1: Single Fault Observability

Cases IV, V and VI include a faulty operational amplifier. The faulty amplifier is detected by observing the differential signals U, V and Y. A fault observed at the output of an operational amplifier can only be due to a fault within the amplifier. For example, a fault observed in node U indicates a faulty behaviour of amplifier OA1. Note that the four shorts in the input differential pair discussed in section 3, which affect the input signal, can be identified. This is because they result in the saturation of the circuit amplifiers and the circuit primary outputs are stuck at differential power rails regardless of the input voltage.

Cases I, II and III are all observed at distinct differential nodes. The location of faulty components in case I is illustrated next. A similar analysis can be performed for the location of faulty components in cases II and III. For case I, node J is affected.

It must first be noted that faults in oppositely situated components (R1/R3, R2/R4, R9/R10 and C2/C4) are equivalent from the point of view of the absolute value of the common mode signal J. However, the common mode signal has opposite phase with respect to the differential input for faults of the same value in oppositely situated components. For example, considering a sinusoidal differential input in the circuit of figure 1, figure 6 represents the phase of the signal J for shorts in components R9 and R10.

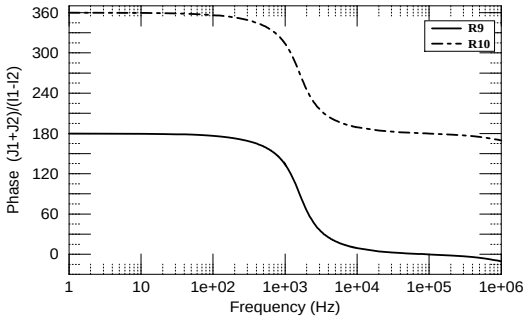

Figure 6: Common Mode Phase

The phase of the common mode signal can be determined from the outputs of the observer. The pass by zero of signal J will cause the error signal to change state from 00 to 11 (for an increasing common mode signal) or from 11 to 00 (for a decreasing signal). The common mode signal will thus produce square output signals from which the phase can be determined.

If the operational amplifiers are not faulty, equations 1 can be used to model them. Considering that a fault is detected if it produces a common mode signal of $[-100, 100]$ milivolts, a computer program is able to calculate the minimum deviations of a passive component which will produce a detectable fault in the observer for a differential input of 1 volt. For a given component P, the set of minimum deviations detected at different frequencies form the **fault detection boundary** of component P. For example, figure 7(a) represents the minimum deviations of R1 with respect to its nominal value R1n at each frequency

that will produce a signal $|J1 + J2| = 100$ milivolts for a differential input of 1 volt.

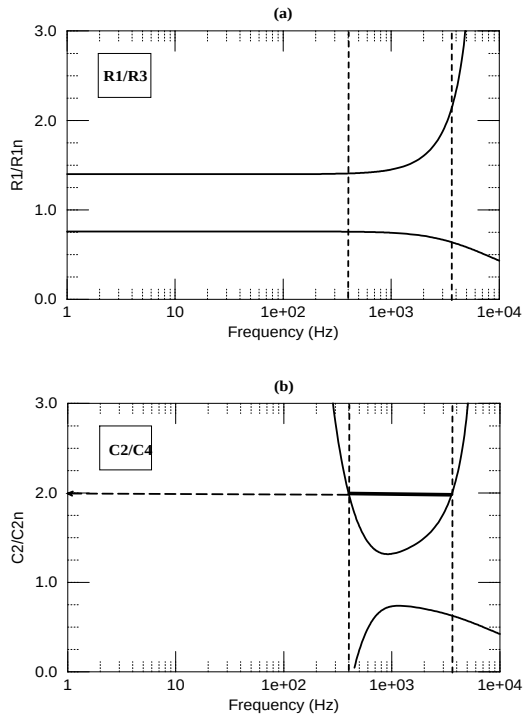

Figure 7: Fault detection boundaries for 1 volt differential input and $|\mathbf{J1} + \mathbf{J2}| = 100$ milivolts. The location of a fault detected in the 400Hz-3600Hz frequency band is also shown.

From figure 7, the soft fault coverage is similar for all components. A fault in a circuit component with nominal value Pn is detected for

$$\left.\begin{array}{l} \frac{P}{Pn} > 1.4 \\ \frac{P}{Pn} < 0.72 \end{array}\right\}$$

(this equally applies to components R2/R4 and R9/R10 which are not shown in figure 7). It must be noted that for higher input voltages the region of undetectability becomes narrower (considering that the amplifiers do not reach saturation).

For the location of a fault, the procedure must first find the range of frequencies for which a fault is detected by the observer. For example, consider a fault which is only detected in the range 400Hz–3600Hz. The region of fault detection is then intersected with the fault detection boundaries as shown in figure 7. From the figure, it is clear, for example, that the fault cannot be located in R1: a fault in R1 detected at 400Hz should also be detected at lower frequencies.

The faulty component is that one for which the fault detection region determined with the analogue observer is limited at both ends by a fault detection boundary. For the example, the fault must be located in component C2 (or C4 according to the phase of the common mode signal) and the deviated parameter has a value of $C2 = 2\ C2n$ according to figure 7(b).

6 Conclusion

This work presents a BIST scheme for a class of analogue circuits which has gained much importance over the recent years for high performance systems. Our approach represents, to our knowledge, the first attempt at efficiently integrating test and diagnosis for fully differential analogue integrated circuits. The testing approach achieves full coverage of hard faults in passive components and a high coverage of hard faults in active components. With respect to soft faults, given the maximum component deviation allowed, it is possible to determine the observer acceptance window and the amplitude of the input test signal which ensure full coverage. A diagnosis procedure for the location of faulty components is presented. In particular, for the location of soft faults in passive components, a new concept of fault detection boundary is introduced. These boundaries allow the location of a faulty passive component and the determination of its defective value.

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