Keynote Speech

The IBM Power PC: Design, Architecture, and Implementation

Abstract
He will begin with an overview of the structure of "Somerset" and its associated design teams. Then the new Power PC chips will be described from three points of view:

1. design point,
2. technology, and,
3. RISC architecture.

A description of the high-level design methodology used for multiple design points will then be given.

He will then describe the tool set used for Somerset, especially some of the critical in-house tools. He will discuss the interaction that has developed between the tools support organization and the design development group. The integration of design tool requirements and design description (at all levels of design) has been a key focal point for Somerset. It is believed that the organization's ability to deliver chips which match their projections is correspondingly determined by their ability to define their requirements at the chip level. He will conclude with a summary of Somerset's accomplishments to date.

About the Speaker
Joseph Hutt is the Head of the IBM VLSI Design Tool Development and Support Organization for the RISC System 6000 Processor Development Group. These support activities include "Somerset" (the Power PC project) as well as other high-performance processor developments.

He has been working with various VLSI design tool development groups within IBM since 1968, and has had to deal extensively with both bipolar and CMOS technologies. He has worked with groups which have developed state-of-the-art physical design software for high performance processors, including those utilizing high-level packaging and large CMOS chips. Recently he spent four years in Mexico setting up the CTS Technology Development Center for the Mexican government. For the past three years, his work has concentrated on the design of CP chips.