An Energy-Efficient CMOS Line Driver Using Adiabatic Switching

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Abstract

We describe a custom CMOS line driver chip and a resonant power supply that can switch eight 100 pF loads at 1 MHz, six times more efficiently than a conventional (CV^2) CMOS solution. We describe the adiabatic charging principle used, which allows a digital circuit designer to directly trade off switching time for increased energy efficiency. Emphasis is placed on evaluating the dissipation overhead for the whole system including the power supply. Measurements confirm the predicted dissipation decrease.

1: Adiabatic switching

Adiabatic switching [1] is a new approach for building low-power digital CMOS systems. It is based on the adiabatic charging principle, which allows circuit switching speed to be directly traded-off against energy dissipation. The major source of dynamic energy dissipation in CMOS circuits is the losses in energy transport between the power supply and the internal nodes of a circuit. Charge is delivered from the power supply at a voltage V and is then later returned to the power supply at voltage 0 (ground). For a signal node of capacitance C, the power supply must deliver a charge CV at voltage V. The power supply then provides an energy QV = CV^2, all of which is dissipated in the resistive elements in the path from the power supply via the signal node to ground. Changing the resistance of the path only affects the minimum charging time and not the energy dissipation.

The adiabatic charging principle states that the dissipation for a given node capacitance and a given voltage swing can, to a first approximation, be decreased to an arbitrary degree by slowing down the energy transport between the power supply and the circuit's signal node. This makes it possible to cycle a signal through a resistance without dissipating CV^2 of energy. The advantage can readily be understood by assuming a constant current source that delivers the charge CV through a resistance R over a time period T. (A similar situation is when a variable voltage source slowly and lin-

early ramps up the voltage to V over the time T.) The dissipation in R is then:

\[ E_{\text{DISS}} = P \cdot T = I^2 R \cdot T = \left( \frac{CV}{T} \right)^2 R \cdot T = \left( \frac{RC}{T} \right) CV^2 \]  \hspace{1cm} (1)

Therefore, a linear increase in switching time T directly results in a linear decrease in the current and a linear decrease in the dissipation. Of all distributions of current over time, the constant-current case gives the lowest dissipation.

Thus, a circuit using adiabatic switching allows a large part of the signal energies to be returned to the power supply. Such energy recovery in electronic circuits is a familiar principle in high-efficiency power supply design [2], and has also been used in other electrical engineering domains such as drivers for electroluminescent displays [4]. This paper presents an application of the same principle to a simple logic circuit.

2: RLC switching

To take advantage of the gains offered by adiabatic charging, not only the logic circuitry but also the power supply must be designed with adiabatic operation in mind. We will first consider the power supply.

The constant-current case described above requires that the power supply generate linear, voltage ramps. Unfortunately, we do not know how to deliver and recover energy at constant current without dissipating more energy in the supply which provides the constant current source. However, as was also observed by Younis and Knight [5], it is possible to efficiently deliver the charge via a sinusoidal waveform using an inductor. Theoretically, the energy dissipation is then increased to [1]:

\[ E_{\text{DISS}} = \xi \frac{RC}{T} CV^2, \quad \xi = \frac{\pi^2}{8} \]  \hspace{1cm} (2)
\( \xi \) is a \textit{shape factor}, due to the fact that the current is delivered to the node sinusoidally rather than at a constant level. The shape factor quantifies the influence of the deviation from the ideal, constant-current charging. Here, \( R \) includes both the switch resistances in the logic circuits and any resistance in the path of the current in the power supply.

The circuitry of an inductor-based power supply may be arranged as in Figure 1. The "tank" capacitance, \( C_T \), is much larger than the load capacitance and is held at half the desired maximum output voltage. Together with the resistance and the "A" switch, the capacitances and the inductance form an underdamped RLC circuit. Provided that the initial voltage on the load capacitance is 0, the voltage will follow an exponentially damped sinusoid with a maximum close to \( V \).

For the circuit to be usable, we need a way to stop the oscillation at the maximum output voltage, and a way to replenish the energy dissipated in the resistances. The first requirement is met by using a single enhancement-mode MOSFET as a switch, marked "A" in the figure, in series with the inductor. The switch is tied once (turned on), for a time \( T = \pi \sqrt{L/C_L} \), to charge the load capacitance, and tied once again to discharge it. The time is chosen in such a way that the voltage on the load capacitance is at its peak when the switch is cut, as shown in Figure 2. At the end of the cycle, energy is injected into the circuit by restoring the initial voltage levels, using the switches marked "B" in the figure. The associated dissipation (caused by the voltage drop across the "B" switches) decreases with decreasing dissipation in the RLC circuit, and is much smaller than the RLC dissipation for reasonable circuit parameters.

The insertion of the "A" switch increases the total resistance in the RLC circuit, and thereby the dissipation per charge-discharge cycle. Assume that the switch is driven by a conventional driver, i.e., all the energy stored on the gate capacitance is dissipated every cycle. If the switch device is made wider, its on-resistance will decrease, and so will the dissipation in its channel; on the other hand, its gate capacitance will increase, and so will the energy spent for driving it. For given values of \( V \), \( C_L \), and \( T \), there is an \textit{optimum} switch device width that minimizes the total dissipation. The optimum width, as well as the corresponding minimum total energy, are proportional to the \textit{square root} of the inverse of the charging time. (Equation (2) does not take the dissipation in the power supply into account.)

It is in principle possible to decrease the power supply dissipation by using a second inductor circuit to drive the gate of the switch of the first circuit. In general, it can be shown [1] that for a cascading of \( N \) such circuits for which the parasitic capacitances are neglected, the total energy dissipation depends on the charging time as:

\[
E_{\min} \sim T^{-(1 - 2^{-N})} \tag{3}
\]

Thus the dependence asymptotically approaches \( T^{-1} \) with increasing \( N \), even though this asymptote is rarely approached in practice because of the relatively large effect the parasitic capacitances have on circuit operation.

3: The ALDC experiment

The logic style used in the adiabatic circuit is heavily influenced by the power supply. With a power supply like the one described above, dual-rail logic is necessary if the capacitive load seen by the power supply is to be constant.

To show that the adiabatic switching principles can be used in practical circuits, and to verify the reduced energy dissipation experimentally, we have designed, fabricated, and tested a simple adiabatic line driver chip (ALDC) [1]. Several properties of the ALDC application make it a good choice.
for an initial demonstration circuit. First, the driven capacitances are relatively large, and the speed requirements are moderate, so the theoretical power savings are considerable. Second, it is a combinational circuit with completely reversible input-output behavior, so none of the inescapable non-adiabatic dissipation associated with information erasure will affect it [3][6][7]. Third, it is a very simple circuit, allowing us to characterize it fully and isolate the non-ideal phenomena.

The ALDC comprises eight differential drivers, each corresponding to Figure 3. It was designed to drive a load of 100pF per line with an efficiency of 95% for 500ns linear ramps. According to the above, the minimum energy dissipation for a full charge-discharge cycle is:

$$E_{\text{adiabatic}} = 2 \cdot \frac{RC}{T} \cdot C \cdot V^2$$  \hspace{1cm} (4)

The classical energy dissipation for the same load and voltage is:

$$E_{\text{classical}} = C \cdot V^2$$ \hspace{1cm} (5)

The requirement of 95% efficiency translates to:

$$\frac{E_{\text{adiabatic}}}{E_{\text{classical}}} = 2 \cdot \frac{RC}{T} = 0.05$$ \hspace{1cm} (6)

This gives the required on-resistance of each transmission gate as 125 \( \Omega \).

In every cycle, one of the complementary outputs of each driver is connected to the adiabatic supply voltage \( V_a \). The dissipation is therefore the same in every cycle. With a supply voltage of 5 volts, the minimum power dissipation according to Equation (4) for the ALDC would be 1mW at 1MHz, compared to 20mW if the eight 100pF lines were driven conventionally (Equation (5)). This should, however, be regarded as a lower limit. Practical considerations will diminish the actual gains. First, we cannot reasonably expect to use the entire cycle for charging and discharging; we need stable periods between the transitions for the inputs and outputs to settle. Second, the power dissipated by the circuit that generates the supply voltage ramp (the "adiabatic power supply" or APS) is overhead compared to the conventional case and must be taken into account when the two approaches are compared. Third, the shape factor \( \xi \) will be larger than one in any real circuit, since the ideal constant-current charging can at best be approximated. Fourth, the idealized, linear components used to derive the expression for the adiabatic power dissipation are usually unavailable for implementation.

Our simplified analysis of the circuit demonstrates the main properties and design compromises, despite neglecting the effects of the non-ideal components. For a better prediction of the dissipation, the non-idealities must be taken into account. First, stray capacitances associated with the load must be included when the effective load capacitance is computed. Second, ringing effects in the inductor and associated parasitic dissipation are unavoidable, although some of the effects may be made arbitrarily small by varying the circuit topology and improving the exact timing of the switch. Finally, the resistances of the RLC circuit are non-linear; however, the effects of the non-linearities can be minimized by appropriately scaling the devices.

4: Measurements

For our experiments, we used 40-pin DIP packaging and a protoboard. This added 80pF of stray capacitance to the circuit plus 80pF of circuit capacitance for the ALDC. For driving eight 100pF loads plus this extra 160pF capacitance, the predicted full-cycle energy dissipation according to Equation (4) is 1.96 nJ. This includes the effect of the stray capacitances at the load side, but no other non-ideal effects are taken into account. The measured dissipation is 2.0 nJ. An additional 0.4 nJ of energy dissipation per cycle is required to drive the gate capacitance of the switch with a conventional driver circuit. The "B" switches are much smaller than the "A" switch, and driving their gates causes negligible dissipation. The total energy dissipation for a full cycle is therefore 2.4 nJ.
When the same load is driven with a conventional circuit, the package and protoboard still yields 80 pF of stray capacitance. Driving 880 pF conventionally to 4.153 V (the voltage reached at the load in our measurement) causes a dissipation of 15.2 nJ, which is 6.3 times more than the energy dissipated by our adiabatic circuit.

It is instructive to consider the distribution of the dissipation over the different parts of the circuit. According to simulations of the test circuit, 51% of the power dissipation is in the ALDC, 29% is in the channel of the FET switch used to time the energy transfer, another 17% is spent driving the switch gate, and 3% is in the parasitic resistance in the inductor. This points out the importance of taking the dissipation of the entire system (including the power supply) into account, not only that of the logic circuit.

5: Conclusion

We have developed techniques for designing simple digital CMOS circuits that transfer charge in a time determined by the period of a time-dependent power source, rather than the RC time constants of the devices themselves. These circuits are shown theoretically to have lower dissipation than conventional CMOS logic circuits, for the same voltage swing, load capacitance, and number of switching events. Although realizing the potential energy savings does require rethinking the design of the power supply as well as the logic circuits, the low-power operation of these circuits is achieved without reducing the signal energies of the circuits and without requiring a special VLSI fabrication process for the ICs. We are currently working on extending the principles to more complex circuits, both sequential and combinational, with the goal of reducing the overhead in the logic circuits and in improving the efficiency of the power supply circuits. So far, none of the practical difficulties encountered have been fundamental limitations.

As a practical experiment, a real device using the techniques described has been designed and prototyped. The device demonstrated a factor of 6.3 increase in energy efficiency at 1MHz, including the overhead of operating the power supply. We are now building a RAM extension board for IBM PC compatible computers using ALDCs to drive the address lines for a bank of commercial-off-the-shelf RAM chips. If successful, this board-level project will lead the way to developing a low-power solid-state disk using adiabatic switching principles.

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7: References


