FPGA architecture and CAD present many problems to the new and experienced FPGA builder. In this panel, we will discuss several open questions. The following short presentations will form the basis for discussion, which will take place with much audience participation.

1 **FPGA Yield Enhancement Through Redundancy**

This is the idea that one could make larger FPGAs if one could eliminate defective logic and routing by replacing it with spare parts on the chip. Since FPGAs are already configurable, this seems like a natural notion. These two speakers will give their perspectives on this idea:

*John Turner*, Director of Design Engineering, Altera.

*Steve Trimberger*, Manager of Advanced Development, Xilinx.

2 **FPGA Logic Synthesis: Is it a separable discipline from regular logic synthesis?**

Are there FPGA-specific problems to be solved in logic synthesis, or is it only a subset of the general synthesis problem? If so, what broader problem formulation in the literature covers FPGAs? If not, which FPGA-specific problems are not covered by conventional synthesis?

*Rick Rudell*, Synopsys, speaks to the idea that FPGA synthesis is a subset of regular synthesis.

*Jason Cong*, UCLA, speaks to the notion that there are many FPGA-specific synthesis issues.

3 **Methods of FPGA Architecture Exploration.**

The architecture of an FPGA is the function of its basic logic block, the interconnection structure, and all the little nubbly bits that people might throw in. How does an FPGA architect decide what these things should be? There are five ways to measure the goodness of each architecture under consideration:

1. Develop a suite of CAD tools to synthesize for that architecture. “Implement” benchmark circuits on the architecture and, using a model, measure how fast and big it is.

2. Do the design and full-custom layout of the architecture, and see how big and fast it is.

3. Ask the customers if that is what they want, and if so, give it to them.

4. See how well it runs the PREP benchmarks.

5. Develop a theoretical model independent of actual circuit applications and “prove” that the architecture is good or bad.

*Jonathan Rose*, University of Toronto, will speak on methods 1 and 5.

*Telle Whitney*, Principal Architectural Engineer, Actel, will give an industrial perspective.