MOS Transconductor-Based Field-Programmable Analog Array*

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Abstract

An area-efficient technique for implementation of a field-programmable analog array is proposed. The design consists of configurable analog blocks (CABs) that contain op-amps and/or passive elements. The connections between CABs are realized using four-transistor MOS transconductors. The conductance is controlled by varying the gate voltages as defined by either multi-valued memories or external/internal signals. A 1.2 μm CMOS IC with four CABs and 48 transconductors has been fabricated. Several analog circuits including: filter biquad, VCO, precision rectifier, quadrature oscillator, four-quadrant multiplier, square root circuit and sample-and-hold circuit have been successfully prototyped and tested on this IC.

1 Introduction

Field programmable gate arrays for prototyping digital circuits are now commercially available from several vendors. Conspicuously absent in the literature is a field-programmable analog array (FPAA) and perhaps for good reason – many more challenges must be addressed such as bandwidth, linearity, signal-to-noise ratio, frequency response, etc. To address this challenge, we developed one approach to realize a field-programmable analog array [1] that utilized subthreshold current-mode techniques. The reconfiguration for different analog functions and the connections between them were made by pass transistors activated by a set of configuration bits. However, this approach is not appropriate for linear and general analog circuit applications due to the parasitic effects of the pass transistors.

This paper proposes an entirely new approach to the realization of a FPAA for analog circuits that eliminates the effects of parasitics introduced by its inherent interconnection network. At the same time, high linearity, noise immunity and area efficiency are achieved. Figure 1 illustrates the basic idea of a conceptual FPAA. The function of each configurable analog block (CAB) and the connections among CABs are determined by the content of the shift registers which activate the switches in the interconnection network. This IC strategy offers a simplified analog circuit design methodology with the advantages of instant prototyping of various circuit structures (reducing time to market), programmable parameters and CAD compatibility. The configured circuits are also testable since the building blocks in a FPAA can be accessible through the interconnection network such that each block can be tested exhaustively.

2 Circuit Techniques and Architecture of FPAA

2.1 MOS transconductor as switch

Although it is hard to realize an ideal zero impedance switch in MOS technology, it is possible to linearize the switches by replacing each pass transistor with a four-transistor transconductor [2] as shown in Figure 2. The transconductor is in the OFF-state and has no current flow through it when the gate voltages are low. The transconductance \( G_{on} \) in the ON-state is

\[
G_{on} = \mu C_{ox} \frac{W}{L} (V_{g1} - V_{g2})
\]

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where \( v_1, v_2 \) is less than \( \min[V_{g1} - V_T, V_{g2} - V_T] \). When the mobility \( \mu \) is assumed to be constant, the transconductance will be linear with respect to the input voltages \( v_1 \) and \( v_2 \) within the above ranges. In addition, the conductance is also controlled linearly by the gate voltages \( V_{g1} \) and \( V_{g2} \). Based on the above equation, the transistor not only acts as an on/off switch but also as a polarity change switch and variable resistor by applying different gate voltages. Therefore, we can use the four-transistor transconductor as an element in a circuit instead of only being a connection switch. Furthermore, if two transconductors – A and B are cascaded, the transconductance is still linear and the equivalent transconductance \( G_{eq} \) is given by

\[
G_{eq} = \mu C_{ox} \frac{W}{L} \frac{(V_{ga1} - V_{ga2})(V_{gb1} - V_{gb2})}{V_{ga1} + V_{ga2} + V_{gb1} + V_{gb2} - 4V_T}
\]

where \( V_{ga1}, V_{ga2} \) and \( V_{gb1}, V_{gb2} \) are the control voltages for the transconductor A and B, respectively.

2.2 Architecture of the proposed FPAA

Although the transconductor provides linear resistance, the performance of different circuits configured at the transistor level using transconductors is degraded somewhat due to the finite resistance. In order to utilize the resistance efficiently, we propose a block level reconfiguration technique [3]. The blocks, which refer to configurable analog blocks (CABs), consist of either active or passive elements. The connections between different CABs are realized using the four-transistor transconductors as shown in Figure 3. Each line represents a differential wire and the circles represent the transconductors. There are two interconnection networks in the figure which are VRIN (Variable Resistor Interconnection Network) and SCRN (Signal Controlled Resistor Network). The gate voltages of the transconductors in VRIN are controlled by multi-valued memories [4]. The gate voltages in SCRN are controlled by the outputs of the active elements or external input signals. The architecture also includes voltage or current sources which provide reference voltage or current for some applications. When the transconductors between two CABs are turned on, a resistor is made between the two blocks. Therefore, different circuits can be realized using the active or passive elements with different transconductor connections determined by configuration bits stored in shift registers, and different transconductance values which are determined by the values stored in the multi-valued memories. Fully differential op-amps are chosen as the active elements in this design due to the relatively well-established theory and practise of op-amp circuit design.

3 Prototype Implementation

The concept of MOS transconductor based FPAA is verified through prototype implementation. The prototype consists of 4 CABs, a 2x8 SCRN, a 4x8 VRIN with 4 memory refresh circuits (MRC) and a quantized level generator (QLG) which generates quantized levels for the MRC to refresh the multi-valued memories. Only one of the four CABs contains passive elements.

The CAB containing the active element (op-amp) also consists of switched feedback capacitors as shown in Figure 4. By turning on or off the switches, the CAB can be configured as an integrator, op-amp or comparator. The on/off state of the switches is determined by the content of a shift register. The CAB containing passive elements is shown in Figure 5. It consists of a pair of diodes and capacitors which can be either connected to the interconnection networks or disconnected via a set of switches which are controlled by the contents of a 2-bit shift register. Among the 4 CABs, only one of them contains passive elements and the others contain op-amps with associated feedback capacitors.

The transconductor cell inside the VRIN is defined as the resistor/connection cell (RCC) (shown in Figure 6). It consists of a multi-valued memory cell and a four-transistor transconductor controlled by 2-bit shift register. The differential terminals trconout and trconin correspond to the horizontal and vertical differential wires in Figure 3, respectively. The on/off state and the polarity of the transconductor are determined by register 1 and 2, respectively. PMOS transistors with width-length ratio of 2/106 are chosen to realize the transconductor. The voltage output \( V_m \) of the multi-valued memory is mapped to the voltage \( V_c \) required for controlling the conductance of the transconductor.
by a voltage mapping circuit as shown in the figure.

The schematic of the signal controlled resistor cell (SCRC) in the SCRN is shown in Figure 7. The differential input varin is the signal controlled terminals. Depending on a specified application, the gate voltages of the transconductor can be controlled either with or without the level shifters by defining the content of register 3.

The on/off cell used in SCRN consists of a four-transistor transconductor and a two-transistor transconductor [2]. The on/off state of the transconductors is determined by a 2-bit shift register. The two-transistor transconductor has large width-length ratio and is only used as a connection switch.

The prototype is fabricated in a CMOS 1.2 μm, double-poly, double-metal process. Figure 8 shows the die photo of the prototype chip. The die size is 3,136 μm by 2,808 μm and the core size is 1,509 μm by 1,751 μm. Table 1 summarizes some specifications of different cells. The number of configuration bits required is 110 and the power dissipation of the entire chip is approximately 120 mW.

4 Experimental Results

The prototype chip was tested by configuring it with seven different circuits including a filter biquad, a voltage controlled oscillator, a precision rectifier, a quadrature oscillator, a four-quadrant multiplier, a square root circuit and a sample-and-hold circuit. Three of the seven configured circuits will be discussed in the following sections. The configuration starts with loading the configuration bits into the on-board shift registers and then loading the multi-valued memories from external clock signals. After the configuration cycle, the chip is ready to operate.

The CAB with fully differential op-amp was also implemented in a separate chip. Table 2 shows the experimental results of the op-amp.

Figure 9 shows the schematic of a fully differential continuous time biquad filter and its embedding into the FPAA. The filter provides a low-pass and a band-pass output. Different transfer functions can be programmed by adjusting the values stored in the multi-valued memories. The CABs are configured as integrators by connecting the feedback capacitors to the op-amp as shown in Figure 4. By loading different stored values to the multi-valued memories in the corresponding RCCs, different low-pass transfer functions are obtained as shown in figure 10. The signal-to-noise ratio is approximately 66 dB and the total harmonic distortion is 0.526% at 1 kHz with 1.4 V peak-to-peak output.

A four-quadrant analog multiplier can be obtained using one op-amp and one transconductors. In this experiment, both inputs to the multiplier are tied together and, therefore, it becomes a input squaring circuit. Figure 11 shows the schematic and its embedding into the FPAA. The level shifters required in Figure 11a are obtained by programming the SCRC to include a pair of level shifters. Figure 12 shows the experimental results. The output frequency is twice the frequency of the sine wave input.

A simple voltage controlled oscillator (VCO) consisting of an integrator, a multiplexer and a comparator with hysteresis is shown in Figure 13a. When vC is set to a constant level, v1 will increase (decrease) as time increases. As v1 is higher (lower) than the upper (lower) threshold voltage of the comparator, the multiplexer will select different polarities of vC. As a result, v1 and v2 will oscillate with a frequency dependent on the resistance of the multiplexer, the capacitor pair C, the threshold voltages of the comparator and vC. The comparator with hysteresis is realized by an op-amp with positive feedback resistors. The circuit can be embedded into the array as shown in Figure 13b. Figure 14 shows the experimental results.

5 Conclusion

A new field-programmable analog array design is proposed which consists of two crossbar interconnection networks formed by four-transistor MOS transconductors, a multi-valued memory system, arrays of CABs and programmable sources. The proposed design utilizes the connection elements in the interconnection networks as resistors (variable or signal controlled) as well as switches (on/off or polarity change). Die area utilization using the proposed design is higher than that of the previous design presented in [5] since the interconnection net-
works also operate as programmable functional elements. Furthermore, the noise due to the interconnection networks is eliminated by differential signaling. The use of four-transistor transconductors for connections between CABs achieves high linearity, low power dissipation and high flexibility for a wide range of applications. This concept is verified and demonstrated with a prototype chip which consists of 4 CABs, a 4x8 VRIN and a 2x8 SCRN. Different circuits, which include a biquad filter, a simple oscillator, a four-quadrant multiplier, a square root circuit, a full wave rectifier, a VCO and a sample-and-hold, have been successfully prototyped using the FPAA described in this paper.

Table 1: Specifications of different cells in the FPAA

<table>
<thead>
<tr>
<th>Item</th>
<th>Size</th>
<th>registers</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAB (active)</td>
<td>$246.8 \times 296 \ \mu m^2$</td>
<td>1</td>
</tr>
<tr>
<td>CAB (passive)</td>
<td>$187.2 \times 246 \ \mu m^2$</td>
<td>2</td>
</tr>
<tr>
<td>RCC</td>
<td>$190.8 \times 148 \ \mu m^2$</td>
<td>2</td>
</tr>
<tr>
<td>SCRC</td>
<td>$186.4 \times 148 \ \mu m^2$</td>
<td>3</td>
</tr>
<tr>
<td>On/Off Cell</td>
<td>$186.4 \times 148 \ \mu m^2$</td>
<td>2</td>
</tr>
<tr>
<td>MRC</td>
<td>$190.8 \times 562.4 \ \mu m^2$</td>
<td>—</td>
</tr>
<tr>
<td>QLG</td>
<td>$92 \times 562.4 \ \mu m^2$</td>
<td>—</td>
</tr>
</tbody>
</table>

Table 2: Experimental results of the fully differential op-amp with a 38 pF, 1 MΩ load

<table>
<thead>
<tr>
<th>Item</th>
<th>Measured value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unity gain frequency $f_T$</td>
<td>$\approx 3 \ \text{MHz}$</td>
</tr>
<tr>
<td>Slew rate</td>
<td>$\approx 7.5 \ \text{V/μs}$</td>
</tr>
<tr>
<td>Settling time (1% of final value)</td>
<td>$\approx 2 \ \text{μs}$</td>
</tr>
<tr>
<td>Open loop differential gain $A_o$</td>
<td>$&gt; 1000 @ 100 \ \text{Hz}$</td>
</tr>
<tr>
<td>Common-mode gain $A_m$</td>
<td>$\approx 0.23 @ 100 \ \text{Hz}$</td>
</tr>
<tr>
<td>Fully differential output swing</td>
<td>3 V</td>
</tr>
</tbody>
</table>

References


Figure 1: A conceptual field-programmable analog array

![Figure 1](image1)

Figure 2: Four-transistor transconductor

![Figure 2](image2)
Programmable voltage or current source

Signal controlled resistor cell

Memory refresh circuits

Resistor/connection cell

Signal output lines

External signal control lines

Signal input lines

CAB

On/Off switch cell

Row decoder for refresh

VRIN

Figure 3: Architecture for the field-programmable analog array

Figure 4: Schematic diagram of the CAB containing a fully differential operational amplifier
Figure 5: Schematic diagram of the CAB containing passive elements

Figure 6: Schematic diagram of the resistor/connection cell
Figure 7: Schematic diagram of the signal controlled resistor cell

Figure 8: Die photo of the field-programmable analog array prototype chip
Figure 9: (a) Schematic of a fully differential continuous time biquad filter and (b) its embedding into the FPAA prototype.

Figure 10: Low-pass output of the configured biquad filter with different values stored in the multi-value memories (X-axis: 1 kHz/div. and Y-axis: 10 dB/div.)
Figure 11: (a) Schematic of a square (multiplier) circuit and (b) its embedding into the FPAA prototype

Figure 12: Experimental results of the configured multiplier circuit (Upper: input; lower: output)
Figure 13: (a) Schematic of a voltage controlled oscillator and (b) its embedding into the FPAA prototype.

Figure 14: Experimental results of the configured voltage controlled oscillator (Upper: \( v_c \); lower: \( v_2 \)).