FPGA '94

2ND INTERNATIONAL
ACM/SIGDA WORKSHOP
ON
FIELD-PROGRAMMABLE
GATE ARRAYS

Sponsored by ACM Special Interest Group on Design Automation (SIGDA) with support from Actel, Altera, and Xilinx.
FPGA '94

1994 ACM Second International Workshop on Field Programmable Gate Arrays

February 13-15, 1994
Berkeley Marina Marriott
Berkeley, California USA

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Marriott Hotel, Berkeley, CA, USA

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Welcome to FPGA '94!

Field-Programmable Gate Arrays are revolutionizing the business of ASIC design by providing fast turnaround and negligible non-recurring engineering costs. The challenge in FPGA research is to improve their speed and density through architectural and process innovation, as well as finding new CAD synthesis and testing algorithms that can make effective use of the new architectures. The objective of this workshop is to bring together people who are working in the many areas of research that are necessary to make a complete FPGA, and Field-Programmable System. We hope that you find it interesting and exciting.

General and Program Co-Chairs: J. Rose, U. Toronto, A. Sangiovanni-Vincentelli, UC Berkeley

Program Committee

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Sunday February 13, 1994

6:00pm  Registration

7:00pm  Welcoming Reception, Marriott Hotel, Berkeley, CA

Monday February 14, 1994

8:20am  Opening Remarks

Session 1: Field-Programmable Systems

Chair: Chii-Ping Hsu, Quickturn Design Systems

8:30am  High-Speed Emulation of Communication Circuits on a Multiple-FPGA System, K. Yamada, H. Nakada, A. Tsutsui, N. Ohta, NTT, Japan


9:10am  A Fast-FPGA Prototyping System that Uses Inexpensive High-Performance FPIC, D. Brasen, M. Slimane-Kadi, G. Saucier, Institut National Polytechnique de Grenoble/CSI

Posters

9:30-10:00am  Springbok: A Rapid-Prototyping System for Board-Level Designs S. Hauck, G. Borriello, C. Ebeling, University of Washington

Improved Multiple-Way Circuit Partitioning Algorithms, A. Dasdan, C. Aykanat, Bilkent University, Turkey

FPGA Package Partitioning for Performance, D. Brasen, G. Saucier, Institut National Polytechnique de Grenoble/CSI

10:00-10:30am  Coffee & Posters

Session 2: FPGA Architecture

Chair: Jonathan Rose, University of Toronto

10:30am  Routing Architecture for Hierarchical Field Programmable Gate Arrays, A. Agarwal, D. Lewis, University of Toronto


11:10am  A Datapath Oriented Architecture for FPGAs, D. Cherepacha, D. Lewis, University of Toronto

Posters

11:30-12:00am  Reduced Look Up Tables with Increased Functionality, K. Gudger.
Session 3: Technology Mapping I

Chair: Jason Cong, UCLA

1:30pm  Performance Driven Technology Mapping for Lookup-Table Based FPGAs Using the General Delay Model, A. Mathur, C.L. Liu, University of Illinois, Urbana-Champaign

1:50pm  Technology Mapping for Heterogeneous FPGAs, J. He, J. Rose, University of Toronto

2:10pm  Functional Decision Diagrams for Technology Mapping to Lookup-Table FPGA, E. Schubert, U. Kebschull, W. Rosenstiel, Universitat Tubingen, Germany

Posters

2:30-3:00pm  An Efficient Graph-Based Technology Mapping Algorithm for FPGAs Using Lookup Tables, B. Kapoor, Texas Instruments, Dallas

Logic Module Independent Mapping for Table-Lookup FPGAs, U. Weinmann, W. Rosenstiel, Forschungszentrum Informatik an der Universitat Karlsruhe

Use of Binary Decision Diagrams for FPGA Mapping, T. Besson, V.V. Le, S. Tixier, G. Saucier, Institut National Polytechnique de Grenoble

State Assignment Selection for FPGAs and CPLDs, H. Belhadj, A. Fortas, G. Saucier, Institut National Polytechnique de Grenoble

On the Lookup-Table Minimization Problem for FPGA Technology Mapping, A. Farrahi, M. Sarrafzadeh, Northwestern University

3:00-3:30pm  Coffee & Posters

Session 4: Field-Programmable Analog Arrays and Yield-Enhancement

Chair: Bahram Ahanin, Altera

3:30pm  MOS Transconductor-Based Field-Programmable Analog Array, G. Gulak, E. Lee, University of Toronto

3:50pm  High Speed Field Programmable Analog Array Architecture Design, E. Pierzchala, M. Perkowski, Portland State University

4:10pm  A Novel Approach to Defect Tolerant Design for SRAM Based FPGAs, J.L. Kelly, P.A. Ivey, University of Sheffield, England

Posters

4:30-5:00pm  FPGA with Selfrepair Capabilities, S. Durand, C. Piguet, Swiss Fed. Inst. of Tech.
8:00-10:00pm PANEL:
Open, Closed, Untouched, Irrelevant and Unprofitable:
Questions Worth Pursuing in FPGAs

Field-Programmable chips and systems are a new field with a great deal of promise. Many people have been actively working on many aspects of Field-Programmability for a few years now, and have come to various opinions about what is important. In this panel, we will discuss exactly what is worth looking at in the FP domain, what should be given up as solved, what has never been attacked, what should never be attacked, and whether or not any of these make anyone a profit. A sample of potential issues:

**CAD:**
- Is Lookup Table Technology Mapping for area solved or can we expect important new developments?
- What kind of technology mappers are needed - what cost models, what architectures?
- Should placement specific to FPGAs be addressed?
- Is routing for FPGAs well-solved? For all possible architectures?
- Will anyone solve multi-FPGA partitioning in a reasonable way? Is it solvable?
- Should there be more effort on PAL-based (CPLD-type) FPGA synthesis

**Architecture:**
- Are their architectural dimensions that need to be explored: e.g. hierarchy, heterogeneity, special purpose architectures?
- How should architecture be attacked? With goals of achieving x2 speed, x2 density?
- Is yield-enhancement through redundancy and repair a viable approach?

**Analog:**
- Is a Field-Programmable Analog Array a reasonable thing to try and build?

**Custom Computing Machines:** will there ever be the perfect “compiler” or will users have to be Digital Design Engineers?

There are many different perspectives to take on these questions: those of FPGA silicon vendors, CAD vendors, FPGA users, ASIC users, and University researchers. Each has a different view of what makes an issue important: the cost of an FPGA is all that is important to some while the intellectual challenge of a new idea is the “goal” function for others. The time frame is also relevant: will the solution to this problem help the field as it is now, or 2, 5, 10 or 20 years from now? For companies, the answer to this last question depends on the state of their funding and/or revenue. For academics, it depends on which granting agency is being addressed.

This will be a panel with audience participation. Each issue will be assigned a proponent and a
devil's advocate. Either one will make the initial presentation, to be rebutted by the other. This will open the discussion for speakers from the floor.

Wednesday February 15, 1994

Session 5: FPGA-Based Computing Architectures and Paradigms
Chair: Duncan Buell, Supercomputing Research Centre

8:30am  Mesh Routing Topologies for FPGA Arrays, S. Hauck, G. Borriello, C. Ebeling, University of Washington

8:50am  Programming the Hawaii Parallel Computer, A. Lew, R. Halverson Jr., University of Hawaii

9:10am  Unifying FPGAs and SIMD Arrays, M. Bolotski, A. DeHon, T. Knight Jr., MIT

Posters  Placement and Routing
Chair: David Marple, Crosspoint

9:30-10:00am Algorithms for FPGA Switch Module Routing, M.D.F. Wong, S. Thakur, S. Muthukrishnan, The University of Texas at Austin

On Minimizing Clock Skew During FPGA Placement, M.D.F. Wong, K. Zhu, The University of Texas at Austin

Switch Bound Allocation in Timing-Driven Routing of FPGAs, M.D.F. Wong, K. Zhu, The University of Texas at Austin

10:00-10:30am Coffee & Posters

Session 6: Applications of FPGAs
Chair: Stephen Trimberger, Xilinx Inc.

10:30am  A Field-Programmable Gate Array Implementation of a Self-Adapting and Scalable Connectionist Network, A. Ferrucci, M. Martin, T. Geocaris, M. Schlag, P.K. Chan, University of California, Santa Cruz

10:50am  Taking Advantage of Reconfigurable Logic, B.K. Fawcett, Xilinx Inc.

11:10am  A Variable Precision Multiplier for Field Programmable Gate Arrays, M. Louie, M. Ercegovac, University of California, Los Angeles

Posters

11:30-12:00am Space Efficient Neural Net Implementation, M. Gschwind, V. Salapura, O. Maischberger, Technische Universität Wien

Implementation of a Local Controller for the Reconfigurable Machine Using the
Xilinx's 4005 FPGA, S.S. Erdogan, N. Kuo, A. Wahab, Nanyang Technological University, Singapore

LUNCH 12:00 - 1:30

Session 7: Partitioning and Technology Mapping
Chair: Ewald Detjens, Exemplar

1:30pm
Area/Pin-Constrained Circuit Clustering for Delay Minimization, M.D.F. Wong, H. Yang, The University of Texas at Austin

1:50pm
Min-Cut Replication for Improved Partitions, J. Hwang, Quickturn Design Systems & Stanford.

2:10pm
Using Encoding for Functional Decomposition with Application to Look Up Table Architectures, R. Murgai, R. Brayton, A. Sangiovanni-Vincentelli, University of California, Berkeley

Posters

2:30-3:00pm
A Technique for Synthesizing Data Part Using FPGAs, M. Balakrishnan, A.R. Naseer, A. Kumar, Indian Institute of Technology Delhi, India

Vertex Ordering in Partitioning-Based Fitter for an Application Specific EPLD Device, M. Jeske, T. Gao, A. Coppola, Portland State University

RTL Synthesis System Using FPGA Macro Bloc Capabilities, M.C. Bertrand, A. Mignotte, O. Khalil, G. Saucier, Institut National Polytechnique de Grenoble

3:00-3:30am
Coffee & Posters

Session 8: Placement, Routing and Timing Modelling
Chair: Sinan Kaptanoglu, Actel

3:30pm
A New Approach to FPGA Routing Based on Multi-Weighted Graphs, G. Robins, M.J. Alexander, University of Virginia

3:50pm
A Simultaneous Placement and Global Routing Algorithm for Symmetric FPGAs, N. Togawa, M. Sato, T. Ohtsuki, Waseda University

4:10pm
Fast Delay Estimation in Segmented Channel FPGAs, M. Chew, J-C. Lien, Actel Corp.

Posters

4:30-5:00pm
Timing Modelling for Antifuse Based FPGAs, N.S. Nagaraj, P. Krivacek, M. Harward, Texas Instruments Inc., India

Computational Complexity of 2-D FPGA Routing for Arbitrary Switch Box Topologies, Y-L. Wu, S. Tsukiyama, Chuo University, Japan