Session V-10:
Formal Semantics of VHDL: Practical Need or Academic Pleasure? (Panel)

Chair: Franz J. Rammig, CADLAB, Paderborn, Germany

This panel will bring together experts representing external and internal views of the issue from the academic, vendor and user community.

Panelists:
E. Berger, Universita di Pisa, Italy;
Dominique Borrione, IMAG/ARTEMIS, Grenoble, France;
Stanley J. Krolikoski, Compass Design Automation, Rochester, MN, USA;
Gerry Musgrave, AHL Abstract Hardware Ltd., Uxbridge, United Kingdom;
Carlos Delgado-Kloos, Universidad Politecnica de Madrid, Spain;
M. Payer, Siemens AG, Munich, Germany