The ever increasing complexity and size of electronic systems is demanding new and faster techniques to produce automatic test pattern generation and fault simulation at level of abstractions other than the conventional gate level. This session deals with techniques using behavioral and switch levels.

Speeding up Test Pattern Generation from Behavioral VHDL Descriptions Containing Several Processes
  L. Vandeventer and J.F. Santucci

Algorithms for Behavioral Test Pattern Generation from VHDL Circuit Descriptions Containing Loop Language Constructs
  L. Vandeventer and J.F. Santucci

Testability Analysis and Improvement from VHDL Behavioral Specifications
  Xinli Gu, Krzysztof Kuchcinski, and Zebo Peng

VHDL Switch Level Fault Simulation
  Christopher A. Ryan and Joseph G. Tront