Session V-08: VHDL and Synthesis (II)

Chair: Eugenio Villar, University of Cantabria, Santander, Spain

This session offers a range of papers which extend VHDL-based synthesis towards system design: the first paper addresses HW/SW codesign, the second paper considers interface synthesis from exact timing specifications in VHDL, and the third paper introduces a VHDL-based method for protocol merging.

The Role of VHDL within the TOSCA Hardware/Software Codesign Framework
Donatella Sciuto, Stefano Antoniazzi, Alessandro Balboni, and William Fornaciari

Timing Preserving Interface Transformations for the Synthesis of Behavioural VHDL
P. Gutberlet and Wolfgang Rosenstiel

Wolfgang Ecker, Manfred Glesner, and Andreas Vombach