Session V-07: VHDL Simulation

Chair: Jacques Rouillard, ESIM, Marseille, France

The papers in this session address several aspects of VHDL simulation: development and architecture of VHDL simulators, efficient coding guidelines, application-specific use of VHDL.

Static Analysis for VHDL Model Evaluation
    Mirella Mastretti, Alessandro Balboni, and Mario Stefanoni

Automotive Databus Simulation Using VHDL
    Karen Hale

Distributed Simulation for Structural VHDL Netlists
    Werner van Almsick, Wilfried Daehn, and David B. Bernstein

A New Flexible VHDL Simulator
    Arlet Ottens, Henk Corporaal, and Wilco van Hoogstraeten