Session V-06: From VHDL to Formal Verification

Chair: Dominique Borrione, IMAG/ARTEMIS, Grenoble, France

From a behavioral specification the need to formally verify a practical implementable solution is vital. This session offers a range of approaches which are viable practical with results that act as a catalyst for further work.

Formal Verification of Behavioural VHDL Specifications: A Case Study
Félix Nicoli and Laurence Pierre

(V)HDL-based Verification of Heterogeneous Synchronous/Asynchronous Systems
Hans Eveking

Petri Nets as Intermediate Representation between VHDL and Symbolic Transition Systems
Gert Döhmen

Computing Binary Decision Diagrams for VHDL Data Types
Ronald Herrmann and Hergen Pargmann