Session V-05:
Why Extend VHDL to Analog?
(Panel)

Chair: Jean-Michel Berg, CCI/MCC, Meylan, France

The VHDL hardware description language was primarily designed for the modeling of digital devices. During the 1992 restandardization of VHDL, it was recognized that, among other changes, expanding the language to handle analog designs was worthwhile. Due to the overwhelming number of requirements already under consideration for enhanced digital functionality, the 1076 standardization committee elected to create a VHDL-A subPAR 1076.1 to deal with the problem of adding analog to VHDL. Other initiatives, such as MHDL and proprietary languages, have been developed in the meantime. The debate aims to show how complementary or competitive those initiatives are and to establish whether or not the VHDL extensions are still a valid proposition.

Panelists:
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