Session V-04: VHDL and Synthesis (I)

Chair: Sabine März, Siemens AG, Munich, Germany

This session combines three papers covering semantics and techniques for behavioral synthesis from VHDL. The first paper extends typical high-level synthesis subsets towards interacting concurrent processes, the second paper introduces a scheduling method relying on wait statement motion, and the third paper presents an approach to transforming VHDL behavioral descriptions to descriptions easily handled by high-level synthesis.

Synthesis of VHDL Concurrent Processes
   Petru Eles, Marius Minea, Krzysztof Kuchcinski, and Zebo Peng

Scheduling of Behavioral VHDL by Retiming Techniques
   N. Wehn, J. Biesenack, Peter Duzy, T. Langmaier, M. Münch, Michael Pilsl, and S. Rumler

A Transformation for Integrating VHDL Behavioral Specification with Synthesis and Software Generation
   Frank Vahid, Daniel D. Gajski, and Sanjiv Narayan