Session V-02: Semantic Models for VHDL

Chair: Serafin Olcoz, TGI S.A., Madrid, Spain

The need to cope with ever increasing complexity of systems makes greater demands in the semantics of VHDL standards. This is leading to rigorous formal semantics to enable extensive proofs to be offered to the community. The papers embrace algebra based models to achieve their goals.

The Semantics of Behavioral VHDL ‘93 Descriptions
Wolfgang Mueller, Egon Börger, and Uwe Glässer

A Process Algebra Interpretation of a Verification Oriented Overlanguage of VHDL
Catherine Bayol, Bernard Soulas, Dominique Borrione, Fulvio Corno, and Paolo Prinetto

Proof Theory and a Validation Condition Generator for VHDL
Luis Sánchez Fernández, Peter T. Breuer, and Carlos Delgado Kloos