Session D-17: ATPG for Delay Faults

Chair: Kurt Antreich, Technical University of Munich, Germany

The first paper of this session discusses the tradeoffs between the gate delay and path delay fault model. Focused on path delay faults, two new ATPG algorithms will be presented. In addition the final paper addresses the test of redundant circuits.

Tests for Path Delay Faults vs. Tests for Gate Delay Faults: How Different They Are
Andrzej Krasniewski and Leszek B. Wronski

RESIST: A Recursive Test Pattern Generation Algorithm for Path Delay Faults
Karl Fuchs, Michael Pabst, and Torsten Rössel

BiTeS: A BDD based Test Pattern Generator for Strong Robust Path Delay Faults
Rolf Drechsler

Testing Redundant Asynchronous Circuits by Variable Phase Splitting
Luciano Lavagno, Antonio Lioy, and Michael Kishinevsky