Session D-16: Formal Verification

Chair: Luc Claesen, IMEC, Leuven, Belgium

This session presents a number of formal specification and verification methods based on different basic formalisms: higher order logic theorem proving, process algebras, and Petri nets. These are illustrated with applications to pipelined processors, arithmetic units and parallel controllers.

Formal Verification of Pipeline Conflicts in RISC Processors  
Ramayya Kumar and Sofiène Tahar

An Automatically Verified Generalized Multifunction Arithmetic Pipeline  
Matthias Mutz

Formal Specification and Simulation of Instruction-Level Parallelism  
Edwin A. Harcourt, Jon Mauney, and Todd Cook

An Efficient Verification Algorithm for Parallel Controllers  
Krzysztof Bilinski, E.L. Dagless, Jonathan Saul, and Janusz Szajna