Advanced Simulation and Modeling Techniques for Hardware Quality Verification of Digital Systems

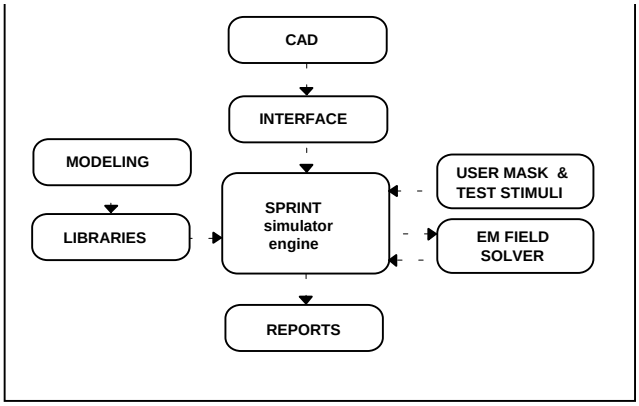

Figure 1: PRESTO simulation flow.

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Abstract

The fast evolution of electronic systems combines high density of components, fine pitch PCB, MCM technology, very fast edge rates in components and large scale integration technique to produce higher operating speeds and system complexity. Signal Integrity (SI) and Electromagnetic Compatibility (EMC) are more and more becoming major issues concerning hardware quality of modern systems. This matter makes it difficult to apply traditional software analysis tools. In this paper, we will discuss software that takes a new approach to the simulation problem with a strong connection between this software and measurement equipment to provide component models.

1. Introduction

The fast evolution of electronic systems combines high density of components, fine pitch PCB (Printed Circuit Board), MCM (Multi Chip Module) technology, very fast edge rates in components and large scale integration techniques to produce higher operating speeds and system complexity. Todays, hardware designers have to face a new set of constraints. First of all, good signal integrity becomes a major goal everywhere in the system. Issues like signal reflections, crosstalk, and switching noise must be controlled and kept below assigned thresholds at the various interconnection levels of electronic apparatus. Timing distribution and synchronisation also play a fundamental role in overall system robustness. ElectroMagnetic Compatibility (EMC) and ElectroMagnetic Interference (EMI) issues also have to be considered because systems must comply with the relevant international standards. New design and test tools are needed to help system designers and validators solving these tough problems.

The ideal tool set would require some important features. First of all, the capability of making fast and accurate characterisations of devices and subsystems with a time resolution compatible to the actual application bandwidth is important. Accurate models should be quickly extracted from these experimental characterisations to perform high fidelity simulations. The simulation engine should support high-complexity situations, typical of complex apparatus, at various levels, such as electrical, behavioural, timing, in order to quickly perform pre- and post-layout analysis of systems. The capability of simultaneously taking into account several effects like signal reflection, crosstalk, switching noise, timing skews and logic behaviour is very important in system quality analysis. A strong integration of modeling techniques, simulation, and system testing is fundamental to fully achieve performance and quality goals of complex apparatus.

It is also necessary to model the entire system, to model all components, including many different types of components whose models come from various sources. Sometimes good simulation models will be readily available, but often modeling is a major challenge. The most

useful software tool will accept models from the sources available to the designer and be able to provide models for the difficult cases. Vendor supplied data (data sheets and IBIS), EM field solver models and SPICE analysis are commonly available, and must be accepted. In some cases, such data are missing or inadequate. In these cases, it is necessary to derive models from measurement. In this paper we will emphasize measurement-based models, since these are especially useful in telecom applications. Finally, a simulation tool must provide accurate, reliable results. Accuracy can be shown by comparison between simulation and measurement of working systems.

In this paper we will present PRESTO^{TM} (Post-layout Rapid Exhaustive Simulation and Test of Operation), a high-performance post-layout quality check software that performs accurate electrical simulations of entire PCBs and MCMs to show signal quality in transmission lines, as well as power and ground plane noise. All nets can be analyzed in the same simulation so that all the parasitic effects are simultaneously taken into account. As shown in Figure 1, PRESTO consists of:

- SPRINT circuit simulator
- automatic netlist extraction from board layout
- electromagnetic field solver
- automatic signal integrity checks (masks&stimuli)
- graphic results processor
- model libraries

2. PRESTO operation

Exploiting the features of SPRINT (Simulation Program of Response of Integrated Network Transients), a fast DSP-based simulator embedded in PRESTO, only few minutes are typically required for the simulation of complex boards at the electrical level.

Figure 2 shows the main results related to a multilayer PCB post-layout analysis.

In low-speed applications, packaging and power supply distribution are in many cases the major causes of operating problems due to simultaneous switching noise. In addition to this, active and passive component modeling becomes a very critical issue for high speed applications. PRESTO also fits the requirements of high-speed designs by allowing the use of accurate models based on TDR (Time Domain Reflectometer) measurements. Models of passive components such as sockets, connectors and cables as well as active parts, such as ICs can be considered for the simulation. PRESTO is able to handle active device models derived from SPICE transistor-level descriptions and process models. A 2D electromagnetic field solver integrated into PRESTO analyzes coupled structures of traces and automatically generates models for an accurate crosstalk simulation. Based on this technique, power distribution and ground planes can be accurately modelled for simulation of switching noise as well.

PREST0: Test Results

Number of Nets : 1931
Number of Components : 1099
Number of Layers : 12
Number of Elements : 92560
Number of Nodes : 60542
Extraction Time :15 min*
Compilation Time : 2 min*
Simulation Time : 40 min*
Total Time : 58 min*
* On a HP750 workstation

Fig.3: PRESTO environment.

A complete compliance analysis of all board signals can be easily performed by comparing waveforms to user-defined masks. The reports are given in terms of mask violation errors, extending the classic concept of signal evaluation on transition times, overshoots, delays, etc. In the figure 3, an example of the PRESTO results is shown.

Sophisticated checks based on signal eye-patterns can be also performed to evaluate features like eye-opening and timing jitter that are especially important for high-speed operation.

With PRESTO, the user can define a set of stimuli to be used to stress the system in the most effective way. Binary sequence patterns can be injected at the input ports to point out faults due to crosstalk, ground bounce and

impedance discontinuities. Specialized classes of tests and their related nets are easily defined.

The translation of board layout data into a simulation netlist is achieved in two separate steps. In the first step, data are extracted from the CAD layout database and translated into an intermediate format from which, in the second step, the actual format required by the simulator is obtained. Two files are needed for the translation, one carrying geometrical information of routed nets and the other with the electrical characteristics of the components. These two files, together with the PCB crossection, are the minimum information needed to start. The translator makes a complete syntax check of the files before starting the translation.

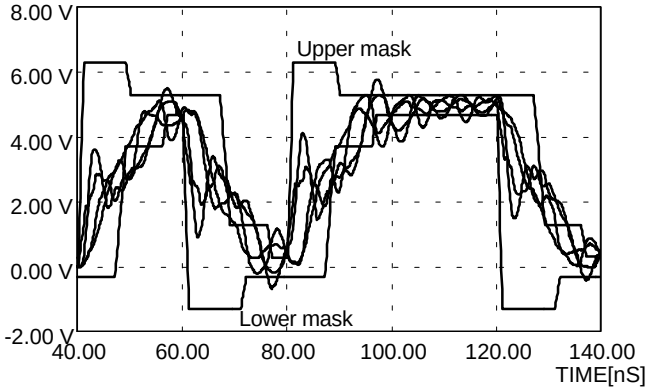

Figure 4. Exhaustive compliance analysis.

Thanks to a powerful geometrical algorithm, PRESTO is able to recognise crosstalk on the same layer or between different layers, in order to build up the input files for the simulator in the next steps. Because of the great number of coupled segments which may be present in high density boards, the algorithm for the crosstalk identification allows the user to define the minimum length for two parallel segments and the maximum distance between them, in order to be considered coupled. The information about the crossection of the board, from which PRESTO creates the crosstalk models, is obtained directly from the layout data base, or it can be specified by the user.

With its embedded graphic environment, the user graphically defines a set of signal masks including upper and lower boundaries that should not be violated by the actual signals (see figure 4). This method allows the user to make precise checks in the interesting portions of signals, ignoring patterns that would not actually affect real operation.

Output reports can be generated both in fully comprehensive ASCII format or graphically. The ASCII reports contain the mask violation errors and their related nets: this is a very useful first-screening tool. Accurate analysis can be performed using the graphical environment in order to identify the causes of the problems found.

3. SPRINT™ simulator

The key to PRESTO's speed and capacity is its simulator SPRINT based on a unique approach especially well suited to digital systems design problems.
SPRINT represents the circuit as a digital wave network, and analyzes it using DSP (Digital Signal Processing) computational techniques. The results is a very fast simulator in which the computation time grows linearly with complexity and which does not suffer convergency problems. By this, the simulator is capable of handling extremely large non-linear circuits.

The algorithm is also very well adapted to simulation of transmission lines and inductors efficiently, as well as other elements. Transmission lines and inductors are very important elements in signal integrity analysis, but can create problems for SPICE.

Models for all types of the circuit and the system components can be obtained easily, eliminating what is often a major bottleneck to simulation. Apart from standard sources, such as EM field solvers, SPRINT models can be derived directly from measurement. The nature of the algorithm makes it easy and natural to derive models from TDR (Time Domain Reflectometer).

Furthermore the accuracy of the simulation can be shown in comparison with measured performance.

To illustrate what SPRINT does, figure 5

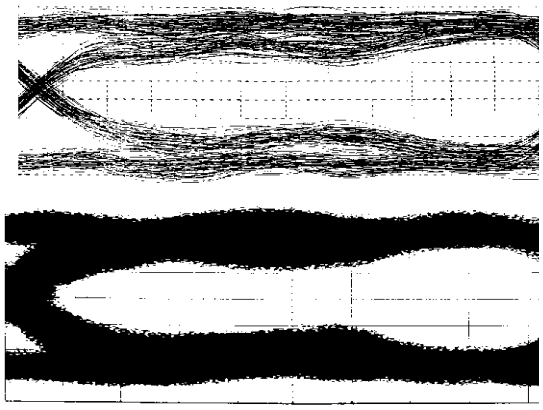

Figure 5: Comparison between simulation and measures of the high-speed multiboard system (155Mbit/s).

shows an example of an eye-diagram generated by simulation of a high-speed multiboard system in comparison to measurement of the actual system in operation. The system is composed of several high-speed boards, in different racks, connected together and to peripheral units. The model for the entire system contains over 50000 elements and is simulated with 32 simultaneous input sequences of 64 random bits each. All signal degradation effects including pin bouncing and timing skews of each crosspoint are taken into account. Simulation time of the entire system with 16.000 time points is about 1 hour on an HP 750 workstation.

The simulation engine maps each element and node into a numerical equivalent which exchanges signals with the rest of the network through its ports. A port of an element is an internal structure carrying the incident and reflected voltage waves (A and B) and the reference impedance Z0 (the voltage is normally referenced to ground).

The simulator calculates the reflected wave at a port by convolution of the incident wave with the time-domain scattering response, i.e., the time domain S-parameter response.

Operating in the time domain enables SPRINT to handle non-linearities, and utilizing the S-parameters directly enables TDR and TDT (Time Domain Transmission) measurement based modeling, so that accurate models of "black box" elements can be derived. The algorithm of SPRINT uses TDR and TDT measurements in a simple, direct and natural way, using a new modeling technique called "Behavioural Time Modeling" (BTM^{TM}).

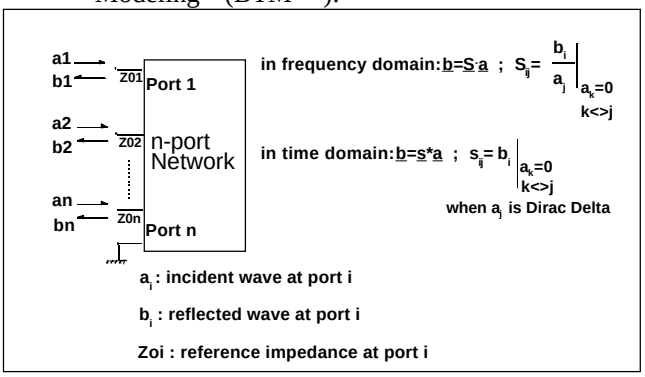

Figure 6: S-parameters representation of networks.

BTM tightly couples the simulator to test equipment. A BTM model consists of an S-parameter characterization of the device under test, derived from TDR/TDT measurement. SPRINT uses these BTM models when:

- great accuracy is desired
- the device is difficult to model by other methods
- special characteristics are desired, such as dispersion in a cable model.

In the next section, we will briefly discuss the basis of BTM modeling, how it relates to TDR and TDT measurements, and in which way the results of BTM can directly be used as SPRINT models.

4. BTM: a new modeling technique

In the frequency domain, scattering parameter step response (S-parameters) is related to incoming and outgoing waves at the port of a network. In general, an n-port network has n^2 S-parameters associated with it. A single reference impedance, Z_o is usually chosen for all ports. For a 2-port linear network, the defining equation at a given frequency is:

$$b_1 = S_{11}a_1 + S_{12}a_2$$
$$b_2 = S_{21}a_1 + S_{22}a_2$$

where a_i represents the incident wave and b_i the reflected wave at port i.

The S-parameters can be interpreted as reflection (S_{ii}) or transmission (S_{ij} $i \neq j$) in matched conditions.

SPRINT modeling is based on the relation of the incident and reflected waves using the time-domain impulse response, represented here as s_{ij}. These are also called the reflection (i=j) and transmission
(i≠j) coefficients. These are directly related to the S-parameter step responses as the time derivative:

$$s_{ij} = dS_{ij}/dt$$

In the time domain, s-parameters relate the incident waves (a) and the reflected waves (b) as follows:

$$b_1(t) = s_{11}(t)*a_1(t) + s_{12}(t)*a_2(t)$$

$$b_2(t) = s_{21}(t)*a_1(t) + s_{22}(t)*a_2(t)$$

where the symbol "*" denotes the time convolution operator and s_{ij} is the generic reflected or transmitted wave in matched

conditions when the incident wave is a Dirac Delta. Figure 6 shows the S-parameter based representation of networks.

For instance, a 2-port linear device is fully characterised by its four S-parameter step responses: $S_{11}(t)$, $S_{12}(t)$, $S_{21}(t)$, $S_{22}(t)$. The device is reciprocal if $S_{12}(t) = S_{21}(t)$. In case of a symmetrical 2-port device, $S_{11}(t) = S_{22}(t)$.

Symmetrical and reciprocal 2-port devices require only two S-parameter behaviour models.

S-parameters impulse responses, $s_{i,j}(t)$ are easily calculated as time-derivatives of step responses $S_{i,j}(t)$. When the DUT (Device Under Test) is connected to an external network, the previous relationship applies between reflected waves b, and incident waves a, at its ports (see figure 7).

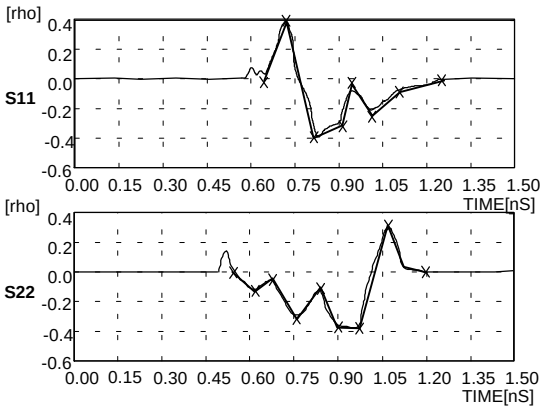

Figure 8: PCB connector model fitting.

From these time-domain impulse responses, SPRINT derives a and b, the incident and reflected waves at each ports; the reflected waves at ports are calculated during simulation by convolution of the incident waves with scattering impulse responses.

Time domain simulations require time convolutions to calculate port signals when BTM model is connected to an external network. A PWL (Piece Wise Linear) fitting of mentioned S-parameters can speed up this convolution process. As it will be shown in the following, for most situations only a few breakpoints are normally required to describe S-parameter behaviour, taking into account the accuracy constraints of digital applications (order some %). This PWL fitting procedure is fully supported by the MCS^{TM} (Model Capture System) of the graphical environment. An example shows how SPRINT directly uses the PWL approximation of the S_{ij} curves in a model description:

```
B2  4  0 S11 = PWL ( 0 0 .1NS .1 .5NS .32 1.5NS .76 3NS 1) Z0=50
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Another important consideration is that non-linear effects of I/O ports of digital devices (ICs) can be modelled with good approximation as purely static (ohmic) non-linearities, superimposed to a linear dynamic response. Simple examples will explain in further detail how to utilize this modeling technique in high speed digital design.

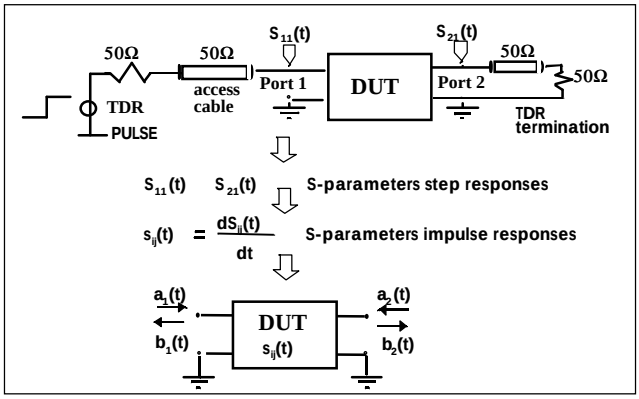

Figure 7: a 2-port device as BTM Black Box.

The behavioural model can be validated through a simulation of measurement set-up, in which a voltage generator (with 50-ohm internal impedance) sends a fast edge (as well as the TDR does) to the modelled device.

The methodology can also be applied to model asymmetrical devices (for example connectors), whose structures are very difficult to treat in terms of lumped parameters because of their discontinuities. A behavioural model is more accurate and easier to build. In this case 3 S-parameters (S_{11}, S_{12}, S_{22}) need to be known because the device is not symmetrical.

Figure 8 shows the reflectometer response for S_{11} and S_{22} and related PWL fitting of a PCB connector. The fitting starts after the first peak, which is the parasitic effect due to the launch cable at the point where it is joined with the device under test. This portion of response can be ignored. Besides BTM, SPRINT supports standard electrical primitives (R, L, C , transmission lines, controlled sources, etc) so that conventional macromodeling techniques can be used or mixed with BTM when necessary.

For fast edge operation, the power and ground distribution planes of PCBs or MCMs cannot be considered as ideal. In fact, the current injected in a particular point of the plane (e.g. by a switching driver or a termination) and its propagating phenomena cause noise which can affect other devices placed on the same substrate. Using a mesh of behavioural blocks it is possible to build up bidimensional models of power and ground planes and take this effect into account. The TDR is an excellent method to validate this technique. Figure 11 shows the comparison between a TDR measurement of a two-layer metal plane (the second plane acts as reference plane) and a simulation in the same configuration. The global behaviour is roughly the typical reflectometer response of a capacitor. A detail of the first section of the graph shows the reflections of the TDR step due to the plane boundaries. It is interesting to point out the very good matching between measurement and simulation. Changing the signal injection point will causes strong modifications of these reflections. Accurate ground and power plane modeling is the fundamental key for the simulation of residual switching noise on multilayer PCBs or MCMs taking the effect of decoupling capacitors into account. Model parameters are optimized through a trial & error technique comparing the actual measure with the simulated TDR response of the model. This process is fast due to short simulation time required.

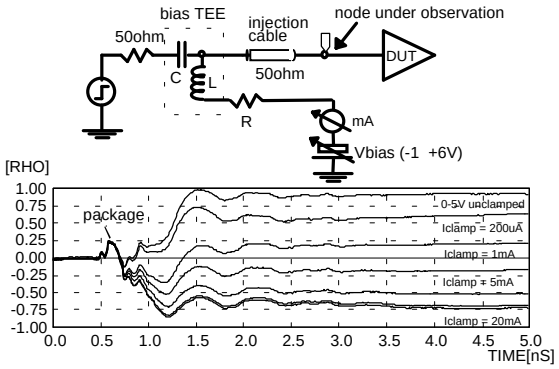

Figure 10: TDR typical setup to model an active input device.

Accurate models of drivers and receivers are vital to good signal integrity analysis. For that reason PRESTO provides behavioural models. These additional models can be created from vendor-supplied information. Models based on data sheets are sometimes less than adequate, but with the IBIS, there is much better way to get relevant data to model active devices, including

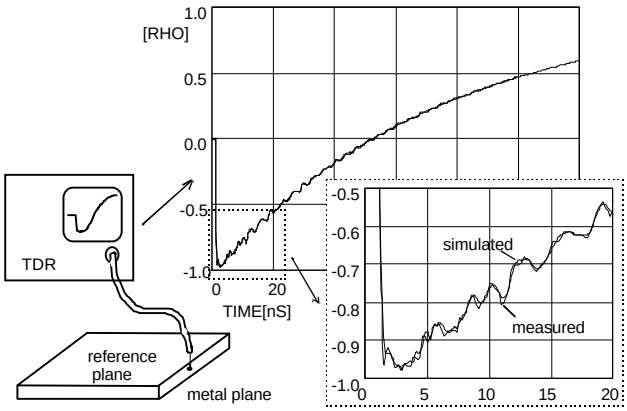

Figure 9: TDR Characterization of Metal Plane.

slew-rate controlled devices. The transformation of IBIS device descriptions is in preparation.

BTM also enables to create active device models based on TDR measurement. These models provide a high level of accuracy, since they contain more information than standard models and also a high level of reliability. TDR measurement accurately models the dynamic behaviour of an input or output in both normal conditions (within the static swing) or in clamping conditions, including the packages effects. Figure 10 shows a typical setup to perform a TDR measurements on an active part. As in Figure 11 a typical CMOS input model is shown. The static characteristics are modeled for both clamping diodes Pvdd and Pgnd and can be obtained by a V/I measurement. The dynamic behavior of the clamping diodes and the input in normal conditions are measured using the TDR. A similar procedure can be followed using a simulative instead of experimental characterization. If transistor-level description of the I/O of active device is available from manufactures, BTM models can be extracted from the TDR setup simulations using analog tool like SPICE, ELDO^{TM}, etc. In this case, the accuracy of results depends strongly on the accuracy of the I/O micromodel available.

5. Conclusions

This paper has shown an application of an integrated measurement and simulation tool offering unique help in design and validation of electronic equipment. Tight integration among wideband time domain instruments, behavioural modeling procedures and a powerful simulation engine is the key feature of this environment. A

great number of actual applications, including design and validation of high-speed multiboard systems, has demonstrated the effectiveness of this approach and its benefits. The features of this tool will be expanded in the near future including EMI facilities like radiated emissions evaluation of PCB traces.

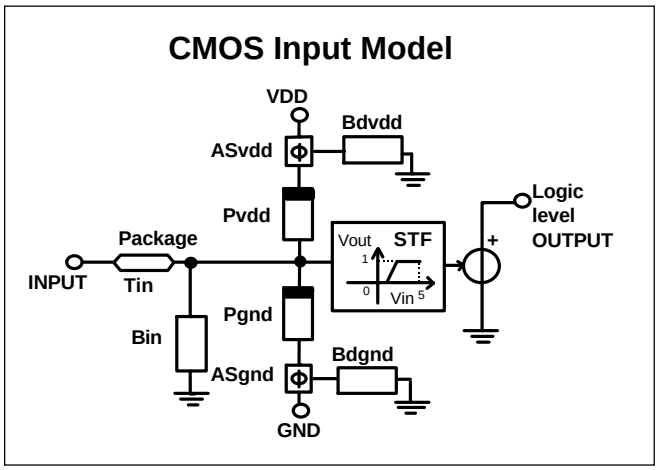

Figure 11: Typical CMOS input model.

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