Session D-04: Specific CAD for FPGA and CPLD Design (Panel)

Chair: Gabrielle Saucier, Institut National de Polytechnique de Grenoble, France

This panel will address the following topics: Which CAD tools are specific for FPGA and CPLD (schematics, simulation, place and route, synthesis)? Who could provide which software? The FPGA and CPLD vendors, the big CAD vendors, dedicated companies? Can place and route tools be provided by CAD companies without the support of the FPGA and CPLD vendors? Does this cause problems? What about synthesis tools? Are they specific? Which quality is required? Is there a need for technology migration tools? At what price should CAD tools for FPGA and CPLD be available on station and PC? Does the pricing issue conflict with quality? Are high level languages mandatory as input for FPGA and CPLD synthesis tools? Will there be a conflict between Verilog, VHDL, Palasm and proprietary languages (HDL from Altera, Minc, and IS Data languages)?

Panelists:
A. Biddle, Actel, Sunnyvale, CA, USA;
D. Kohlmeier, Data I/O, Redmond, WA, USA;
A. Ditzinger, ISDATA, Karlsruhe, Germany;
N. Toon, Altera, Marlow, United Kingdom