Session D-02: Symbolic State Space Exploration and System Timing

Chair: Luc Claesen, IMEC, Katholieke Universiteit Leuven, Belgium

The session starts with efficient OBDD based state space traversal methods that can be used in formal verification and test pattern generation. The second paper describes timing diagrams as a specification for systems. The third paper deals with interface timing verification.

Symbolic Exploration of Large Circuits with Enhanced Forward/Backward Traversals
  Gianpiero Cabodi, P. Camurati, and Stefano Quer

Extended Timing Diagrams as a Specification Language
  Stefan Lenk

Efficient Algorithms for Interface Timing Verification
  Ti-Yen Yen, Wayne Wolf, Al Casavant, and Alex Ishii