Sessions DAC 94

Session 1  Tutorial: Component & Library Management Systems
Session 2  Software & Instruction Set Synthesis
Session 3  Transition Densities for Sequential Systems
Session 4  CAD for Analog and High-Performance Digital Circuits
Session 5A Management of Electronic Design Automation
Session 5B Panel: Executive Perspective and Vision of the Future of EDA
Session 6  Asynchronous Synthesis
Session 7  New Developments in Design for Test
Session 8  Timing Analysis
Session 9  Managing The Design Process
Session 10 Estimation & Synthesis of Memory Structures
Session 11A Intellectual Property
Session 11B Panel: Software Patents and Their Potential Impact on the EDA Community
Session 12 Technology-Driven Routing
Session 13 Panel: ESDA and Design Abstraction: How High is Up?
Session 14 Data-Path Synthesis & Test
Session 15 Topics in Verification and Diagnosis
Session 16 FPGA Partitioning and Optimization
Session 17 Design Implementation
Session 18 BDD Techniques and Formal Verification
Session 19 Panel: Microprocessor Testing: Which Technique is Best?
Session 20 FPGA Placement & Routing
Session 21A Formal Verification
Session 21B Panel: Complex System Verification: The Challenge Ahead
Session 22 Layout and Technology Dependent Synthesis
Session 23 Delay and Self Test
Session 24 Routing for High Performance
Session 25 Panel: Technology Summit - A View from the Top
Session 26 Logic Synthesis
Session 27 Tutorial: Hardware-Software Co-Design
Session 28 Design Representations and Data Structures for High-Level Design
Session 29 Design Methodology
Session 30 Scheduling
Session 31A CAD Algorithms in Non-CAD Problems
Session 31B Panel: DA Algorithms in Non-EDA Applications: How Universal are our Techniques?
Session 32 Fault Simulation and Diagnosis
Session 33 World Class Electronic Design Methodologies I
Session 34 New Ideas in High-level Synthesis
Session 35 Panel: Design Reuse: Fact or Fiction
Session 36 Electrical and Thermal Analysis
Session 37 World Class Design Methodologies II
Session 38 Formal Verification of Systems
Session 39 Interconnect Analysis
Session 40 Circuit Partitioning
Session 41 Panel: Design Automation Tools for FPGA Design
Session 42 Sequential Synthesis
Session 43 New Techniques in Test Generation
Session 44 Discrete Simulation