Session 7: New Developments in Design for Test

Chair: Janak H. Patel

Design for testability is vital to comprehensive testing of large sequential circuits. This session also includes a novel re-synthesis technique for retiming and a new technique for clock grouping.

7.1 IMPLICIT COMPUTATION OF MINIMUM-COST FEEDBACK-VERTEX SETS FOR PARTIAL SCAN AND OTHER APPLICATIONS
Pranav Ashar, Sharad Malik

7.2 AN EXACT ALGORITHM FOR DETERMINING PARTIAL SCAN FLIP-FLOPS
Srimat T. Chakradhar, Arun Balakrishnan, Vishwani D. Agrawal

7.3 RESYNTHESIS AND RETIMING FOR OPTIMUM PARTIAL SCAN
Srimat T. Chakradhar, Sujit Dey

7.4 CLOCK GROUPING: A LOW COST DFT METHODOLOGY FOR DELAY TESTING
Wen-Chang Fang, Sandeep K. Gupta