Panel: Design Automation Tools For FPGA Design

Chair:  Kella Knack - ASIC & EDA Magazine, Los Altos, CA  
Organizer:  Nanette Collins - Exemplar Logic, Inc., Berkeley, CA

Design teams today are challenged with meeting time-to-market and cost constraints while product life cycles decrease and product complexity and functionality increases. Field Programmable Gate Arrays (FPGAs) and Complex Programmable Logic Devices (CPLDs) help meet these challenges by combining the short design cycle of PLDs with the application flexibility and higher integration of gate-array technology.

While PLD and gate-array designers have had a plethora of easy-to-use and proven design tools, the FPGA and CPLD marketplace lagged behind with design tools to address specific demands of these device architectures.

FPGA and CPLD technology requires multi-level optimization techniques not found in PLD design tools and device-specific techniques not found in gate-array design tools. The contrast between the FPGA and CPLD market and the gate-array market is dramatic. FPGA and CPLD design is driven by the variety of fundamentally different device architectures along with price and performance factors. The gate-array design market is driven by the abundance of similar ASIC device libraries.

The variety of new FPGA and CPLD architectures has also confused the user base. Each technology and its accompanying proprietary software requires a steep learning curve. Designers are forced to make up-front decisions-design tools must be purchased for each FPGA or CPLD device. The option to retarget or migrate existing designs is all but eliminated by vendor tools. Further, it is not obvious which technology is best suited for a particular design.

To address these shortcomings, design automation tools specifically developed for the support of multiple FPGA and CPLD device architectures are being made available today. These tools enable designers to implement FPGA and CPLD devices in a variety of ways, including: HDL-based design with either VHDL or Verilog HDL; ASIC prototyping; PAL/PLD migration; and FPGA and CPLD retargeting to ASICs.

The panel session will focus on the wide use of FPGA- and CPLD specific design automation tools, contrasting the difference between these tools with traditional gate-array design tools. It will look at an HDL-based design approach versus the traditional schematic entry. Partitioning will be highlighted, along with protoproduction where CPLDs and FPGAs serve as rapid prototypes for ASIC design. Finally, the business considerations, now a large part of the design cycle, will be addressed.

Panel Members:

John Frediani - Photonics, San Jose, CA  
Gordan Hyland - Philips Labs. Briarcliff, Briarcliff Manor, NY  
Jim Jasmin - Digidesign Inc., Menlo Park, CA  
Tom Reiner - Titan Information Systems, San Diego, CA  
Gabriele Saucier - Inst. National Polytechnic de Grenoble, Grenoble, France  
Steve Trimberger - Xilinx, Inc., San Jose, CA